Model Name : VIUV1
File Name : LA-9761P
BOM P/N:

Compal Confidential

M/B Schematics Document

Intel Haswell with DDR3L
AMD SUN GPU

2012-09-20
REV:0.1

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Title: Cover Sheet			
Size: Custom	Document Number: LA-9761PR01		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 1 of 47		

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Model Name : VIUV1
File Name : LA-9761P
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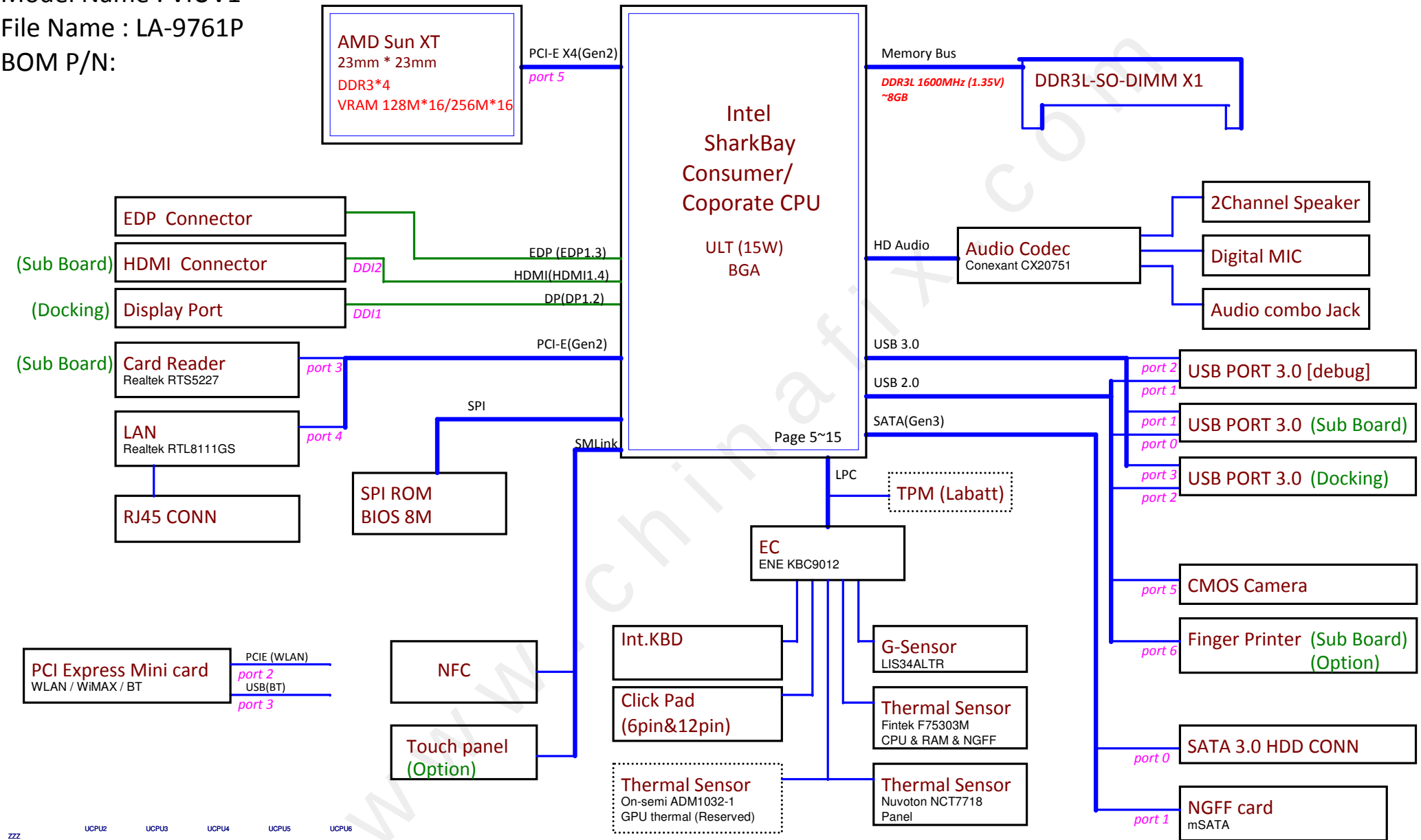

ZZZ
LA9761P
DA_PCB
DA8000XV000

UCPU2	UCPU3	UCPU4	UCPU5	UCPU6
CPU2@ QDJ6_B1_1.0G SA00006FY00	CPU3@ QDJ7_B0_0.8G SA000067H20	CPU4@ QDJ9_B1_1.2G SA00006G100	CPU5@ QDJB_B0_0.8G SA000067010	CPU6@ QDJC_B1_0.8G SA00006EY10

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	~~+3VM~~ ~~+1.05VM~~ (SBA Only)
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

CHECK !

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

CHECK !

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
AMD SUN XT	DIS@
VRAM Option	VRAM@
INTEL UMA	UMA@
CPU OPTION	CPU@
Intel AOAC	AOAC@/nonAOAC@
EMI PART	EMI@
ESD PART	ESD@
HDMI	HDMI@
NFC	NFC@
LAN RTL8111G(S)	LDO@/SWR@
Surge protection	Surge@
TPM	TPM@

EC SM Bus1 address

Device	Address
Smart Battery	

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M Panel Sensor AMD1032ARMZ VGA Sensor AMD1032ARMZ SharkBay ULT AMD SUN XT	

PCH SM Bus address

Device	Address
DDR DIMM0 WALN Touch Pad Security ROM	

PCH SML0 Bus address

Device	Address
NFC	

USB 2.0 Port Table

	USB 2.0 Port	3 External USB Port
	0	USB 3.0 Port (I/O Board)
	1	USB 3.0 Port (MB)
	2	USB 3.0 Port (Docking)
	3	Mini Card (WLAN/BT)
	4	Touch Screen
	5	Camera
	6	FPR
	7	

USB 3.0 Port Table

Port	
1	USB 3.0 Port (I/O Board)
2	USB 3.0 Port (MB)
3	USB 3.0 Port (Docking)
4	

SATA Port Table

Port	
0	HDD
1	NGFF SSD
2	
3	

PCIE Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		Cardreader
5	0	GPU
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SMBUS Control Table

	HOST	VGA	BATT	KB9012	SODIMM	WLAN	PANEL sensor ADM1032	Thermal sensor F75303	VGA sensor ADM1032	CPU Sensor	Touch Pad	Security ROM	NFC
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VLP	X	V +3VLP	X	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VS	X	X	X	X	V +3VS	V +3VS	V +3VS	V +3VALW	X	X	X
SMBCLK SMBDATA	CPU +3VALW	X	X	X	V +3VS	V +3VALW	X	X	X	X	V +3VS	V +3VS	X
SML0CLK SML0DATA	CPU +3VALW	X	X	X	X	X	X	X	X	X	X	X	V +3VS
SML1CLK SML1DATA	KB9012 +3VS	X	X	V +3VS	X	X	X	X	X	V +3VALW	X	X	X

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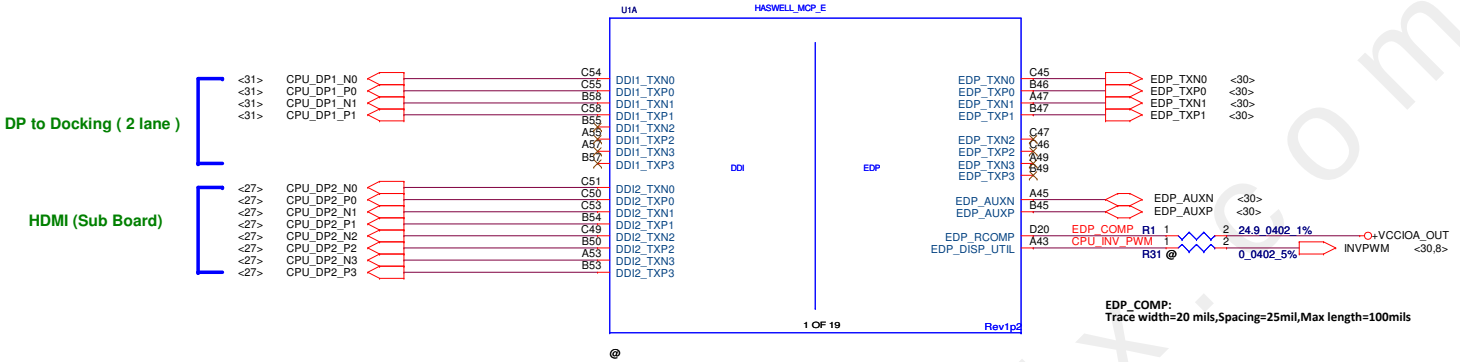
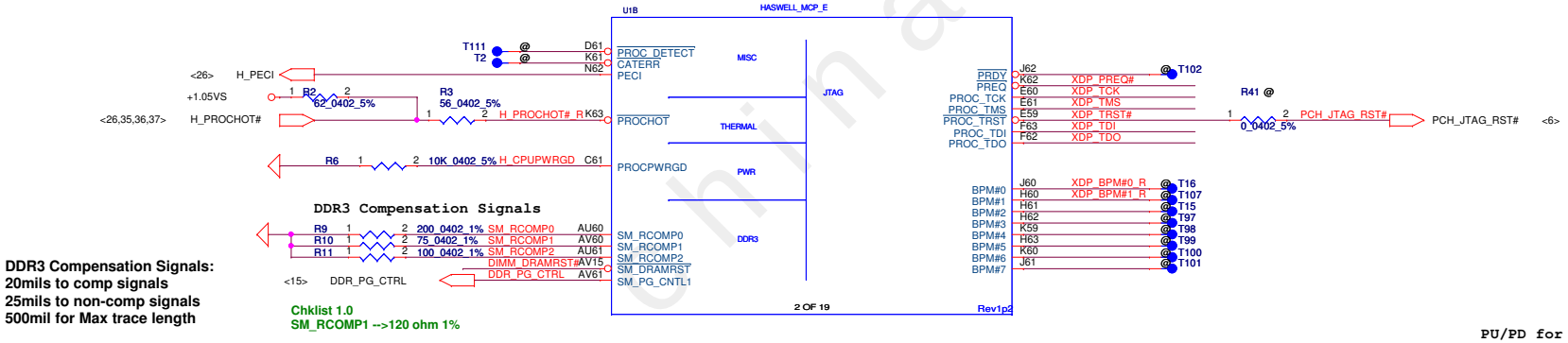


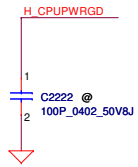


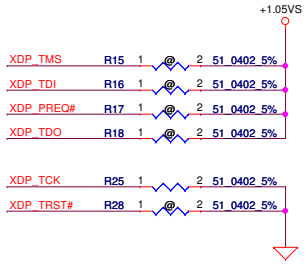
DDR3 Compensation Signals:
20mils to comp signals
25mils to non-comp signals
500mil for Max trace length

Chklist 1.0
SM_RCOMP1 -->120 ohm 1%

PU/PD for JTAG signals

ESD





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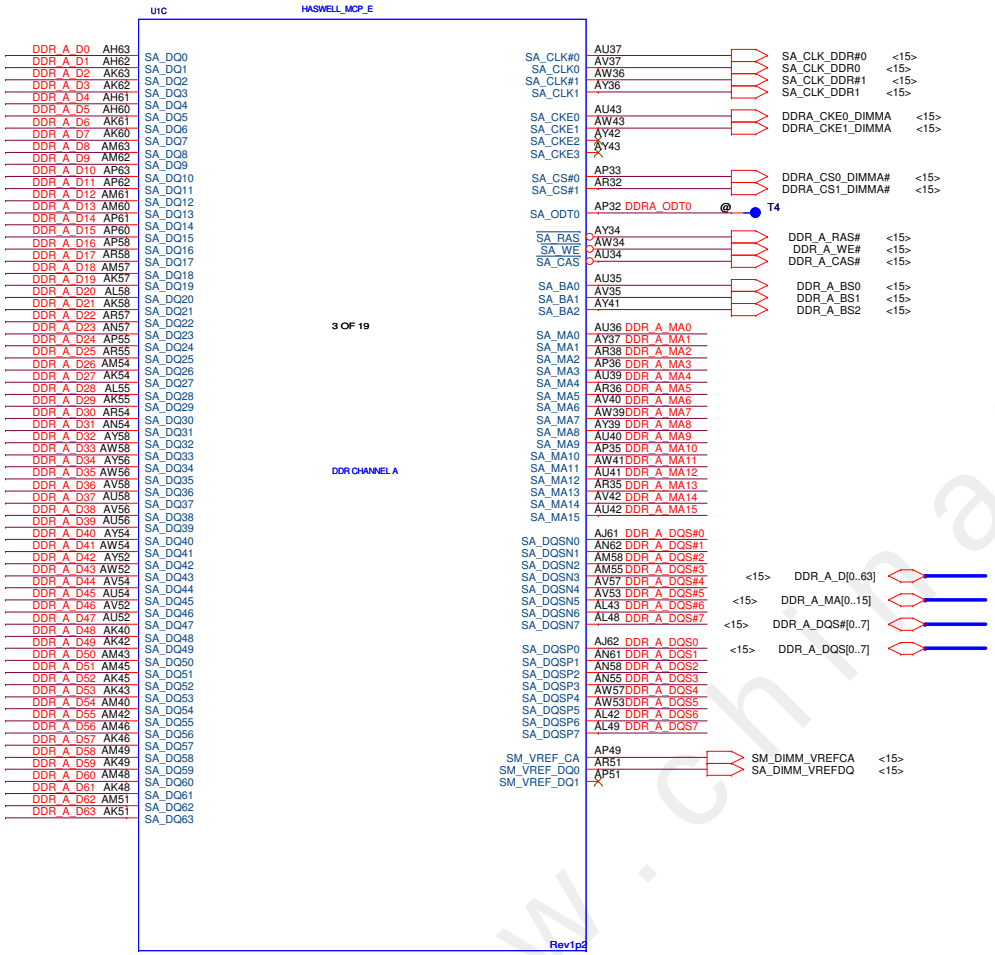

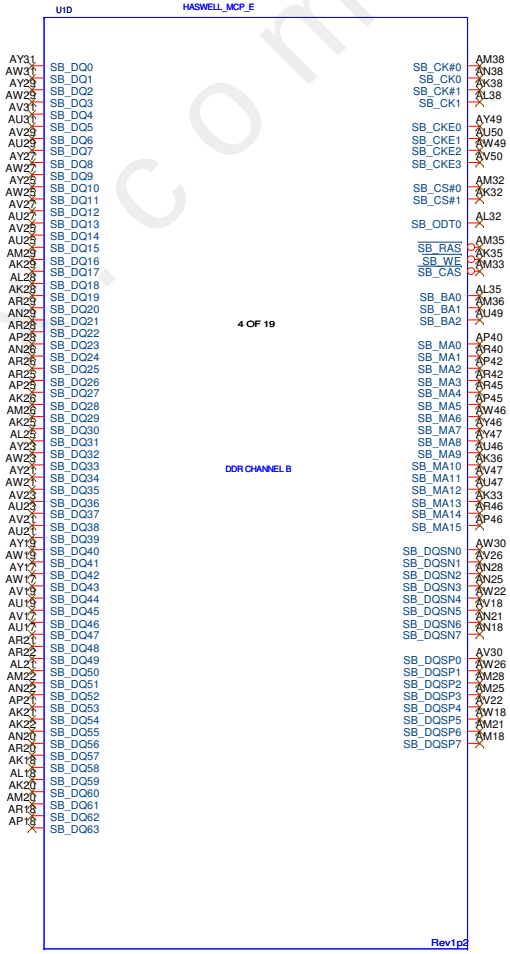

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Issued Date	2011/12/13	Deciphered Date 2012/12/13	Title HSW MCP(2/11) DDRIII

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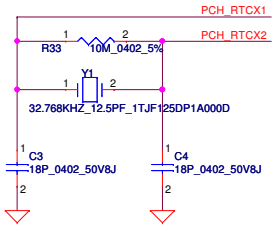
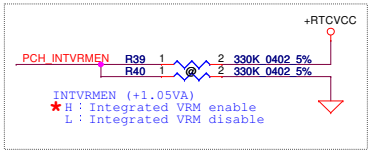
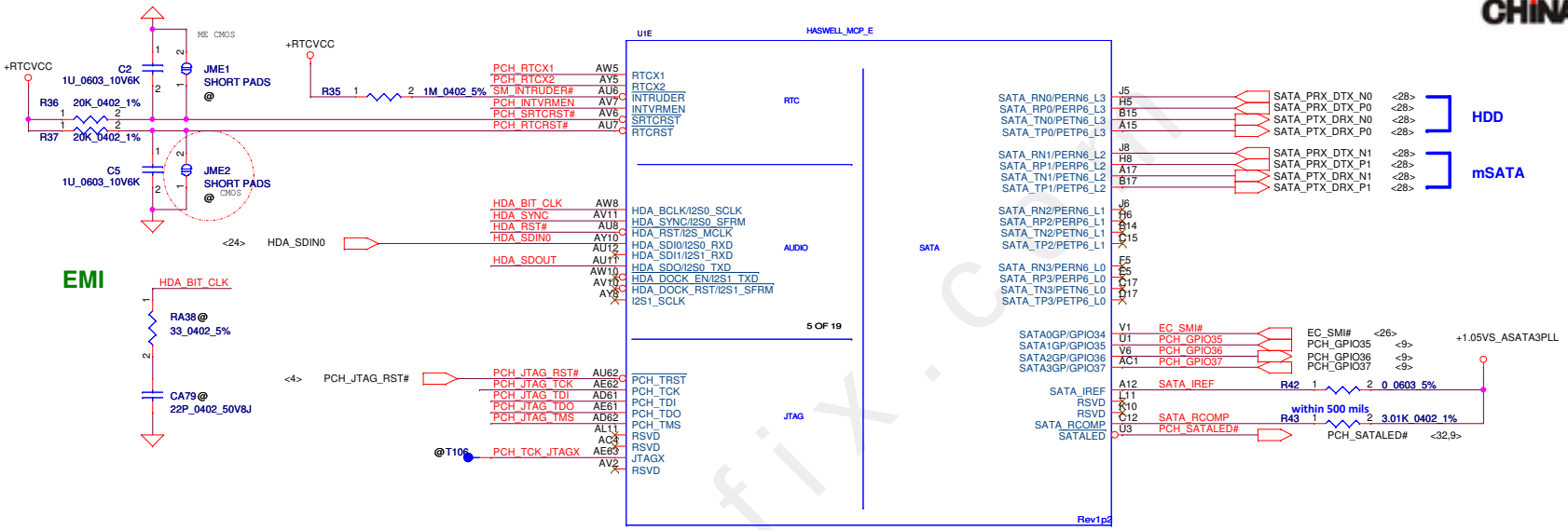


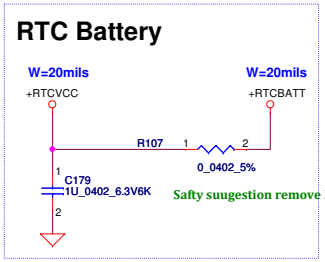
JME2 Short PAD placement to Bottom side.



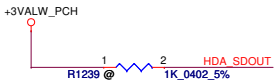


EMI

RTC Battery



Safty suugestion remove EE side ,Keep PWR side



HDA_SDOUT

ME debug mode,this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

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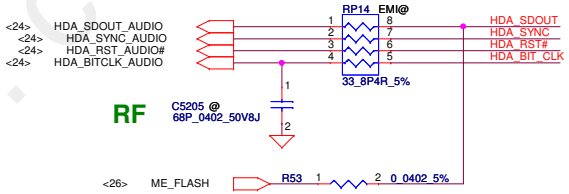
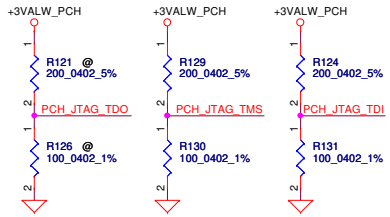
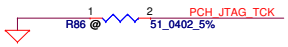
EMI







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Title	HSW MCP(3/11) RTC,SATA,XDP		
Size: Custom	Document Number: LA-9761PR01		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 6 of 47		

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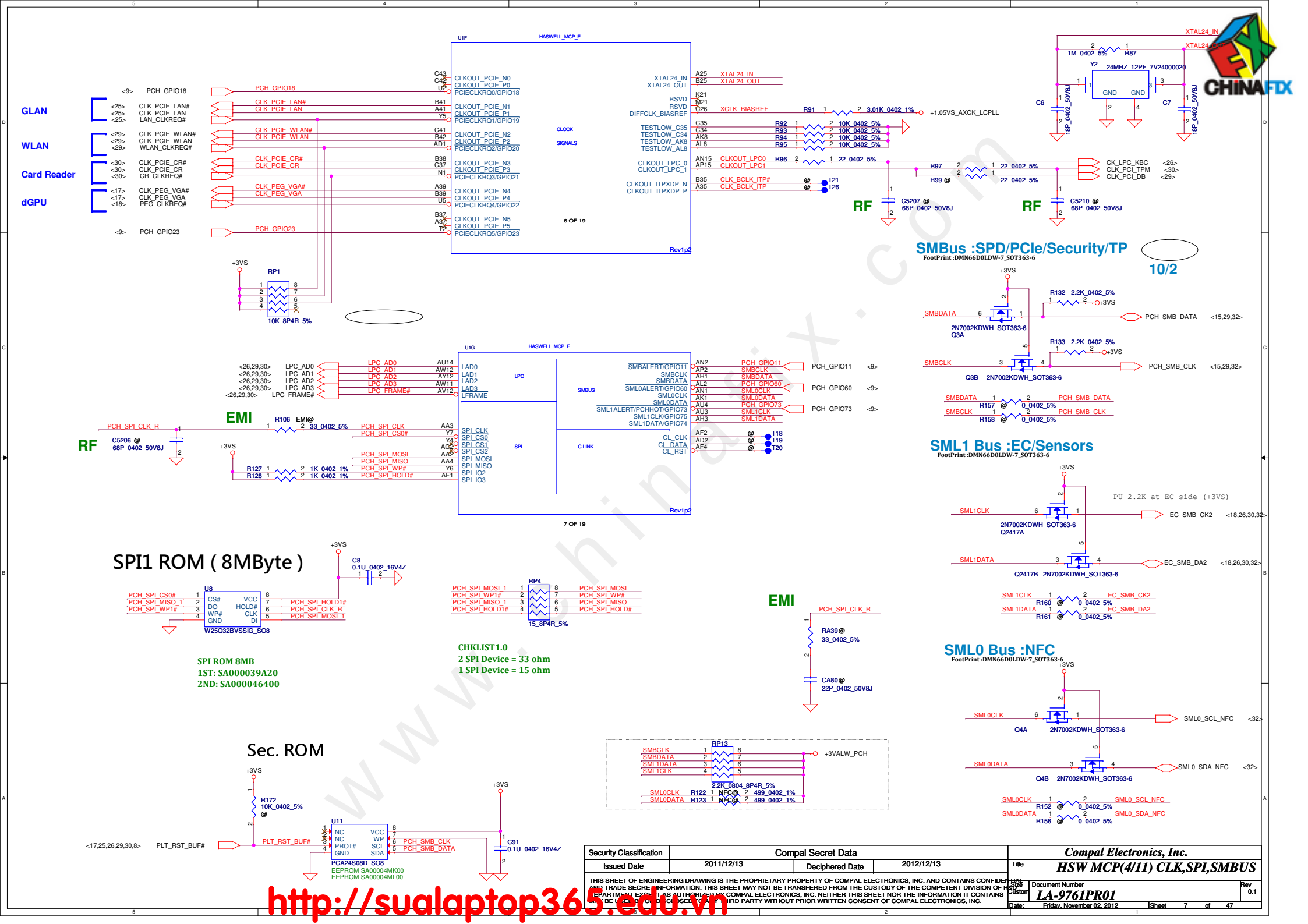

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Compal Electronics, Inc.

Title: HSW MCP(4/11) CLK,SPI,SMBUS

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Note: SUSACK# and SUSWARN# can be tied together if
EC does not want to involve in the handshake mechanism
for the Deep Sleep state entry and exit

CAN be NC ,if not support Deep Sx

DPWROK: Tired toghter with RSMRST#
that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable
H : Enable(DEFAULT)
L : Disable

PCH_PWROK — R146 — APWROK_R (0_0402_5%)

ESD

+3VALW_PCH — R643 200K_0402_5% — D2 — ACIN — AC_PRESENT_R
RB751V-40_SOD323-2

PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)

U1H HASWELL_MCP_E — SYSTEM POWER MANAGEMENT

PCH_GPIO30	R135 0_0402_5%	SUSACK#	AK2	SUSACK
SYS_RESET#		SYS_RESET#	AC3	SYS_RESET
SYS_PWROK		SYS_PWROK	AG2	SYS_PWROK
PCH_PWROK		PCH_PWROK	AY7	PCH_PWROK
		APWROK_R	AB5	APWROK
	C2223 100P_0402_50V8J	PLT_RST#	AG7	PLTRST
	R149 10K_0402_5%			
EC_RSMRST#		EC_RSMRST#	AW6	RSMRST
PBTN_OUT#		PCH_GPIO30	AV4	SUSWARN/SUSPWRDNACK/GPIO30
PCH_GPIO72		PBTN_OUT#	AL7	PWRBTN
PCH_GPIO29	T109@	AC_PRESENT_R	AJ8	ACPRESENT/GPIO31
		PCH_GPIO72	AN4	BATLOW/GPIO72
			AF3	SLP_S0
		PCH_GPIO29	AM5	SLP_WLAN/GPIO29

DSWVRMEN	AW7	DSWODVREN	R134 330K_0402_5% / R139 330K_0402_5%
DPWROK	AV5	DPWROK	
WAKE	AJ5	PCH_PCIE_WAKE#	R148 0_0402_5% → EC_RSMRST# / PCH_PCIE_WAKE# <25,9>
CLKRUN/GPIO32	V5	PCH_GPIO32	→ PCH_GPIO32 <9>
SUS_STAT/GPIO61	AG4	LPCPD#	→ LPCPD# <30>
SUSCLK/GPIO62	AE6	SUSCLK	→ SUSCLK <26>
SLP_S5/GPIO63	AP5	PM_SLP_S5#	→ PM_SLP_S5# <26>
SLP_S4	AJ6	PM_SLP_S4#	→ PM_SLP_S4# <26>
SLP_S3	AT4	PM_SLP_S3#	→ PM_SLP_S3# <26>
SLP_A	AL5	T25	
SLP_SUS	AP4	T110	
SLP_LAN	AJ7	T112	

+RTCVCC

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U1I HASWELL_MCP_E — eDP SIDEBAND / DISPLAY / GPIO

INVPWM	R150 0_0402_5%	EDP_BKCTL	B8	EDP_BKLCTL
ENBKL			A9	EDP_BKLEN
PCH_ENVDD			C6	EDP_VDDEN
DGPU_PWR_EN	R153 0_0402_5%	PCH_GPIO77	U6	PIRQA/GPIO77
DGPU_HOLD_RST#	R151 0_0402_5%	DGPU_PWR_A_EN	P4	PIRQB/GPIO78
		DGPU_HOLD_A_RST#	N4	PIRQC/GPIO79
PCH_GPIO80		PCH_GPIO80	N2	PIRQD/GPIO80
	T27		AD4	PME
PCH_GPIO55		PCH_GPIO55	U7	GPIO55
TS_RST#		TS_RST#	L1	GPIO52
DGPU_PWR_EN	R154 DIS@ 0_0402_5%	DGPU_PWR_I_EN	L3	GPIO54
PCH_GPIO51		PCH_GPIO51	R5	GPIO51
PCH_GPIO53		PCH_GPIO53	L4	GPIO53

DDPB_CTRLCLK	B9	DDI1_CTRL_DATA	→ DDI2_CTRL_CK <27>
DDPB_CTRLDATA	C9	DDI2_CTRL_CK	→ DDI2_CTRL_DATA <27>
DDPC_CTRLCLK	D9	DDI2_CTRL_DATA	
DDPC_CTRLDATA	D11		
DDPB_AUXN	C5	DDI1_AUXN	→ DDI1_AUXN <31>
DDPC_AUXN	B6		
DDPB_AUXP	B5	DDI1_AUXP	→ DDI1_AUXP <31>
DDPC_AUXP	A6		
DDPB_HPD	C8		→ DDI1_DP_HPD <31>
DDPC_HPD	A8		→ DDI2_HDMI_HPD <27>
EDP_HPD	D6		→ EDP_HPD <30>

+3VS
DDI1_CTRL_DATA — R310 2.2K_0402_5%
DDI2_CTRL_DATA — R311 2.2K_0402_5%
DDI2_CTRL_CK — R312 2.2K_0402_5%

DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected
* 1: Port B or C is detected
0: Port B or C is not detected
(Have internal PD)

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R155 0_0402_5% — +3VS
PLT_RST# → U5@ MC74VHC1G08DFT2G_SC70-5 → PLT_RST_BUF# <17,25,26,29,30,7>
R159 100K_0402_5%

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Compal Electronics, Inc.

Title: HSW MCP(5/11) PM,GPIO,DDI

Size	Document Number	Rev
Custom	LA-9761PR01	0.1

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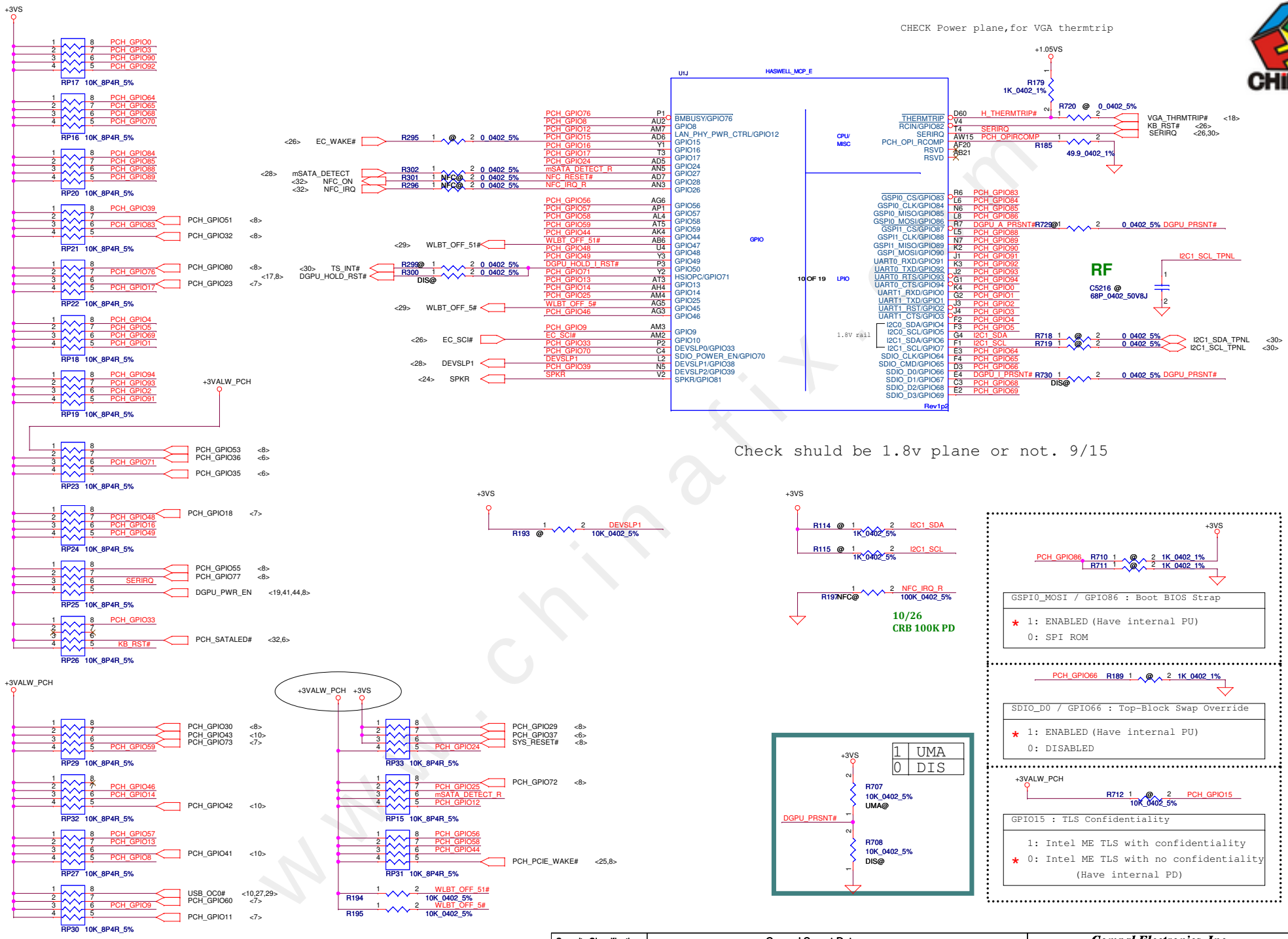

Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	2012/12/13

Compal Electronics, Inc.

Title: HSW MCP(6/11) GPIO,LPIO

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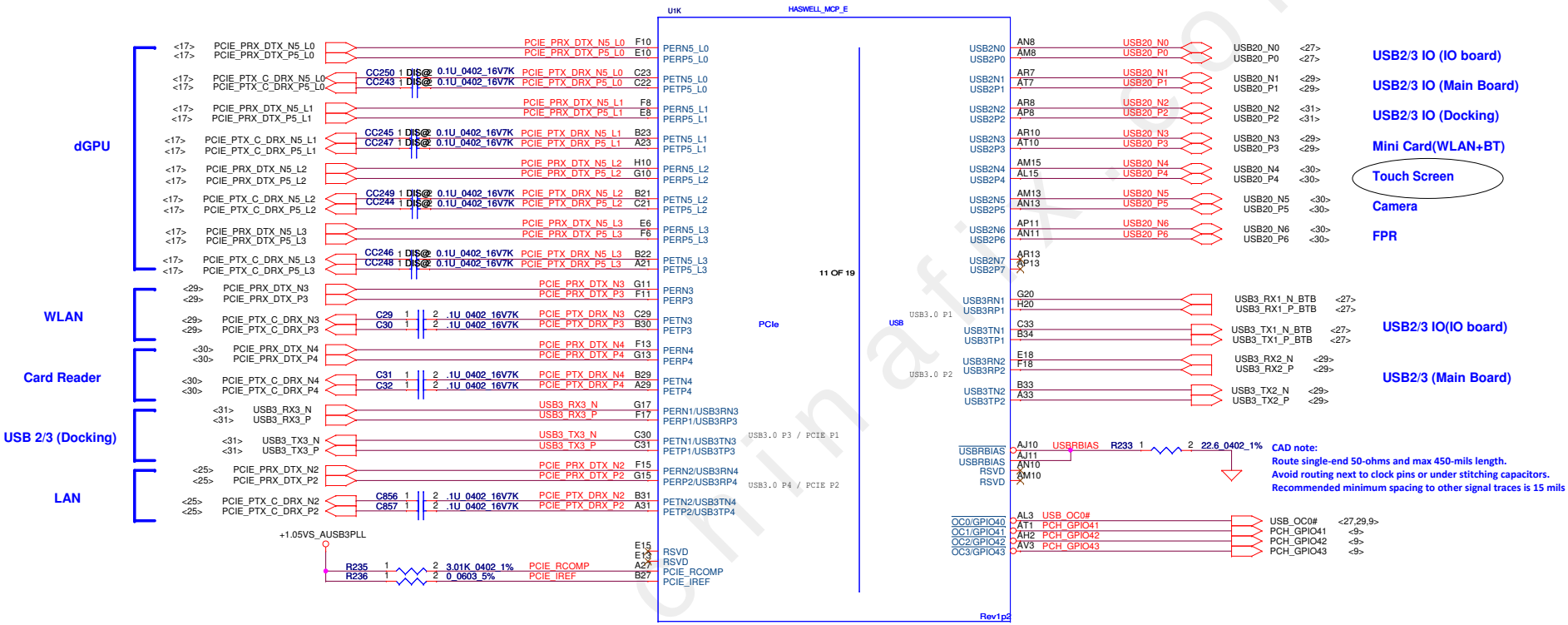

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Issued Date	2011/12/13	Deciphered Date 2012/12/13	Title HSW MCP(7/11) PCIE,USB

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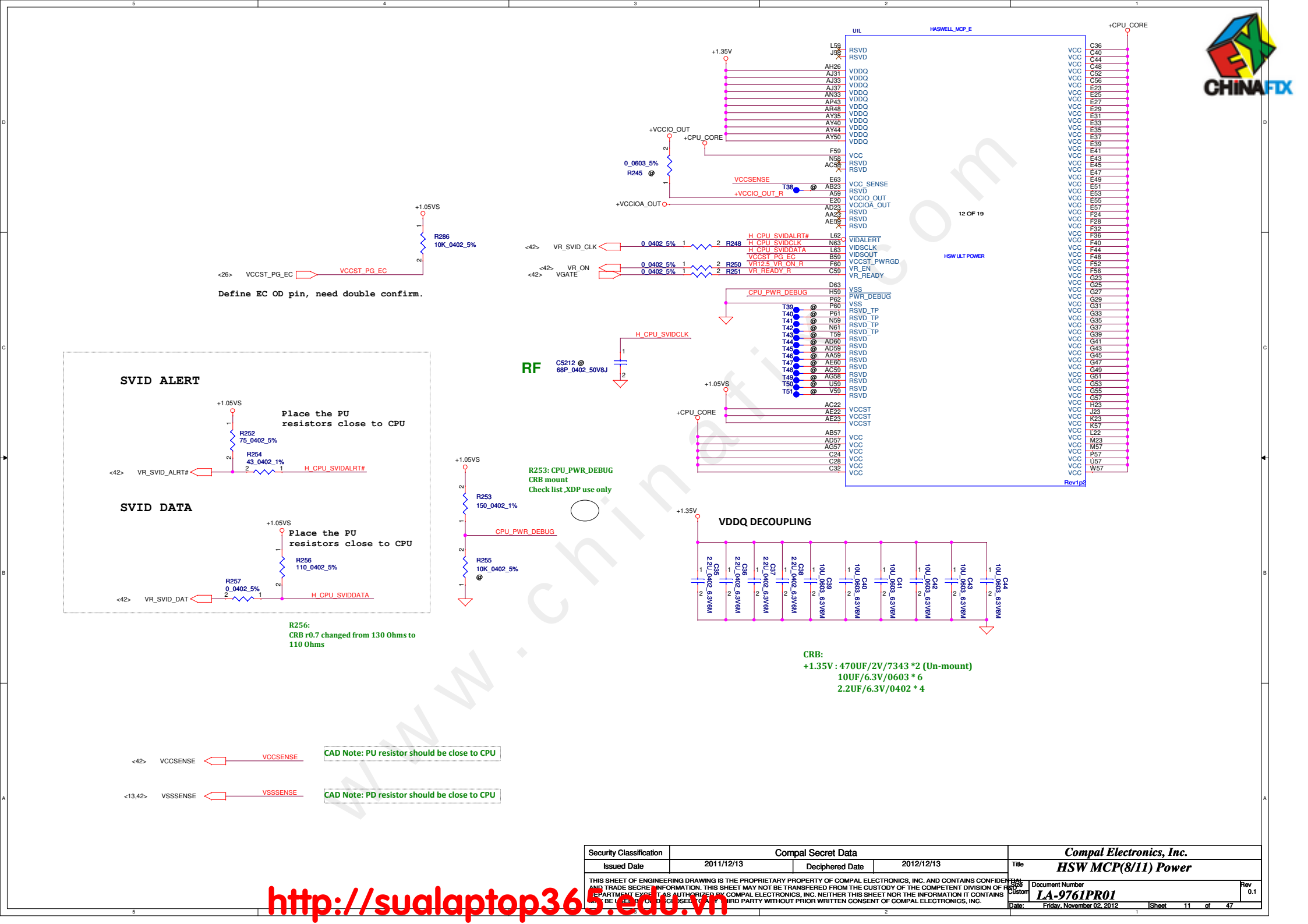

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Compal Electronics, Inc.			
Title	HSW MCP(8/11) Power		
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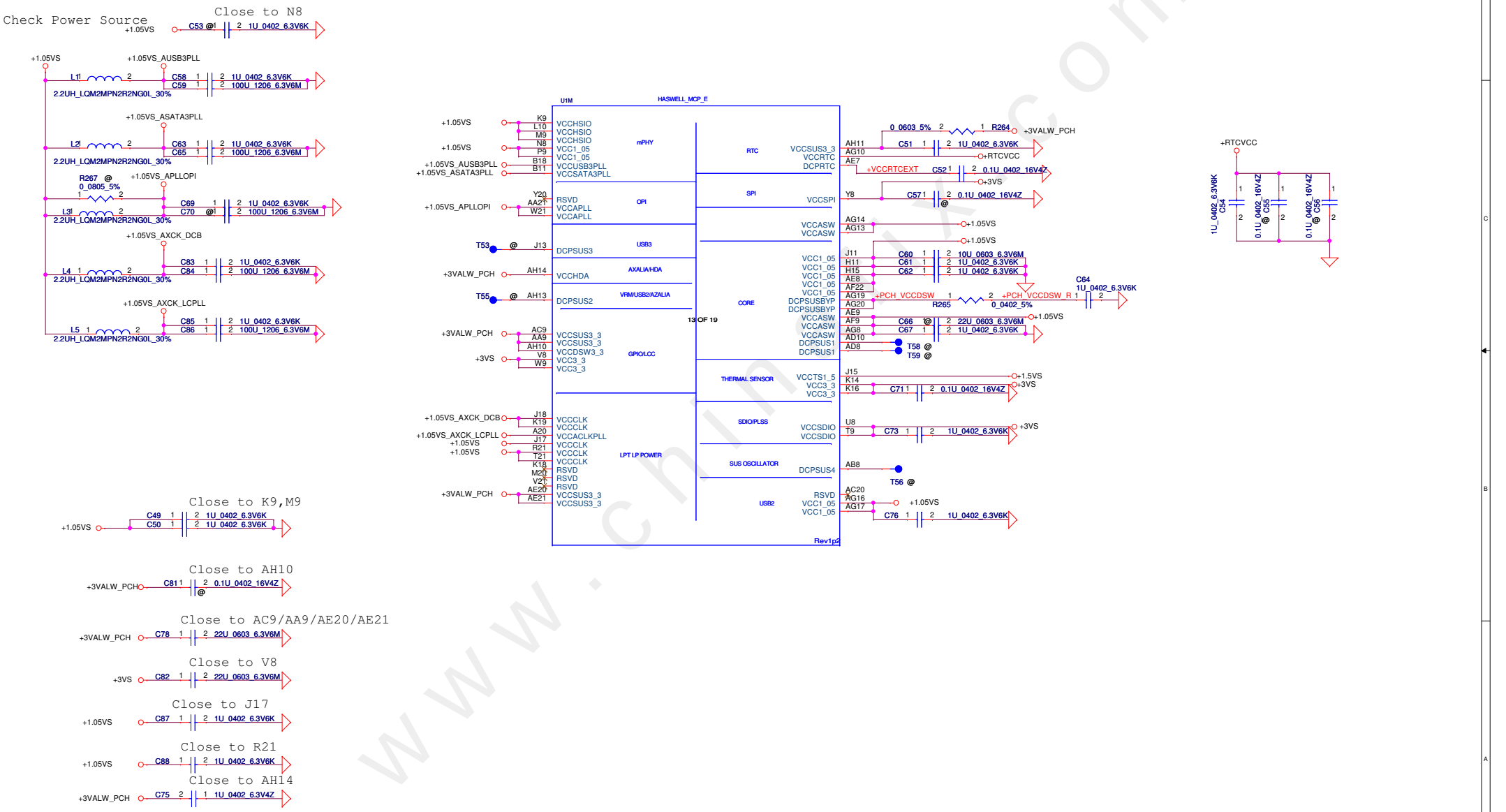

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Title	HSW MCP(9/11) Power		
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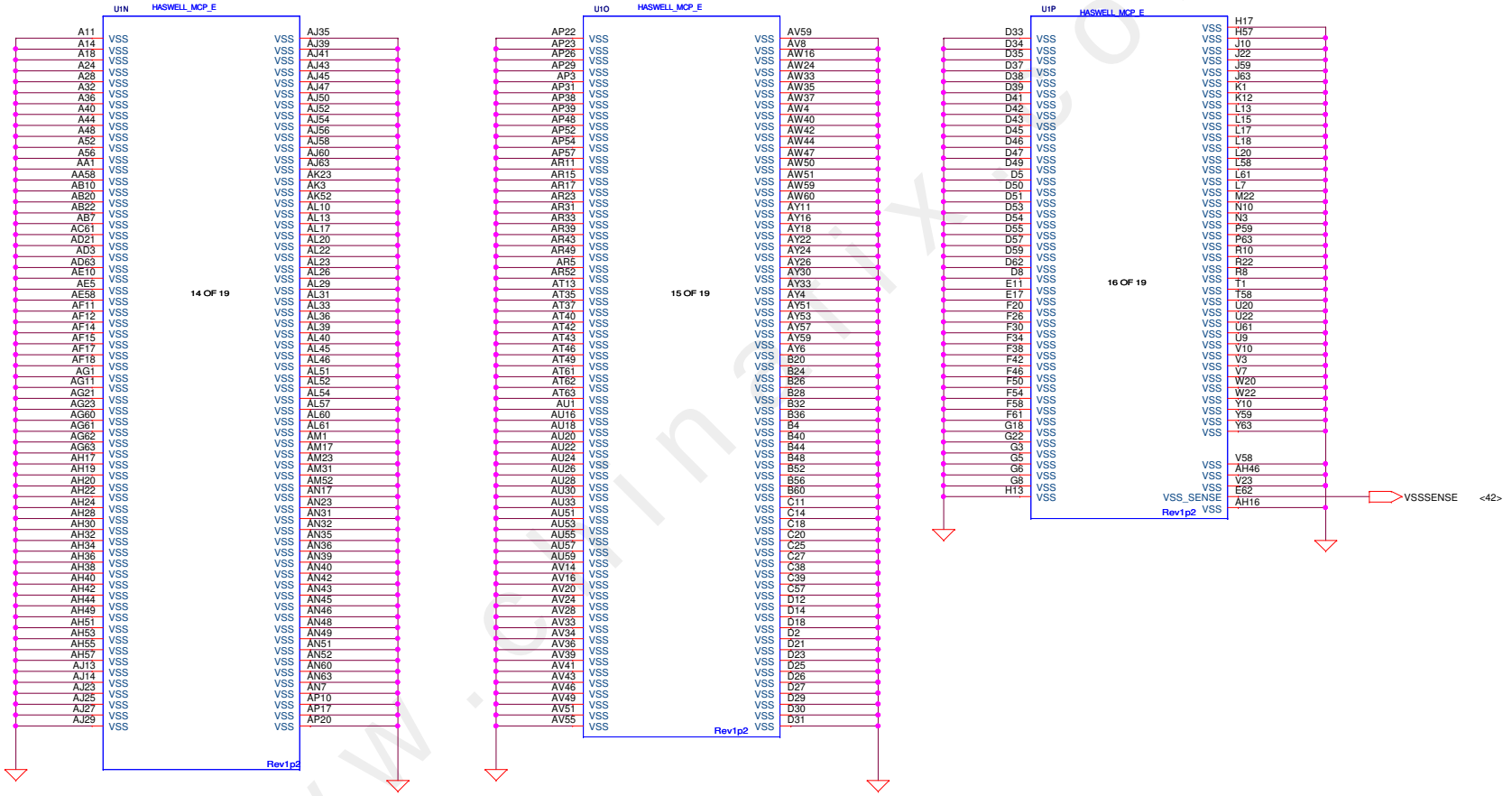

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Title	HSW MCP(10/11) GND		
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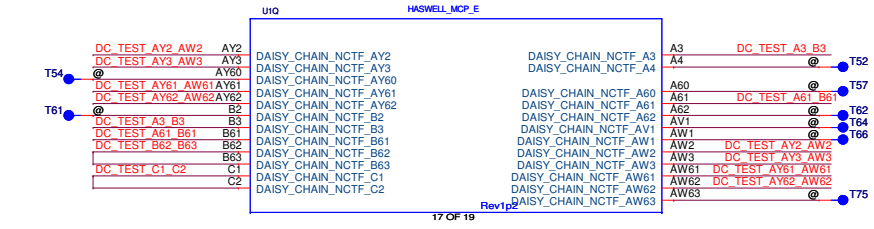
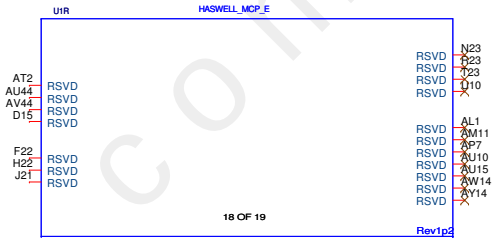
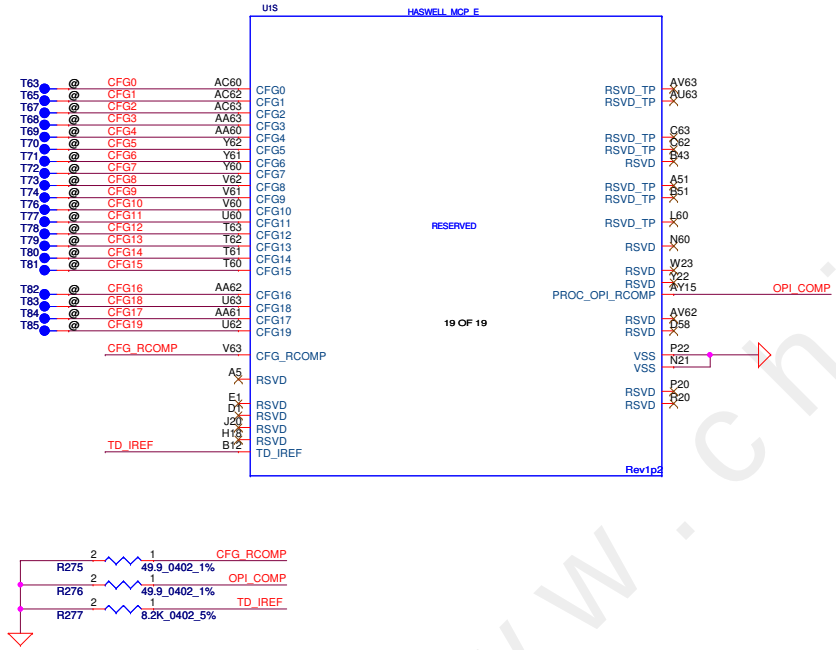
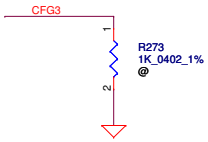


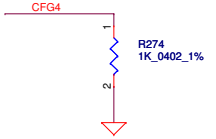




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title	HSW MCP(11/11) RSVD		
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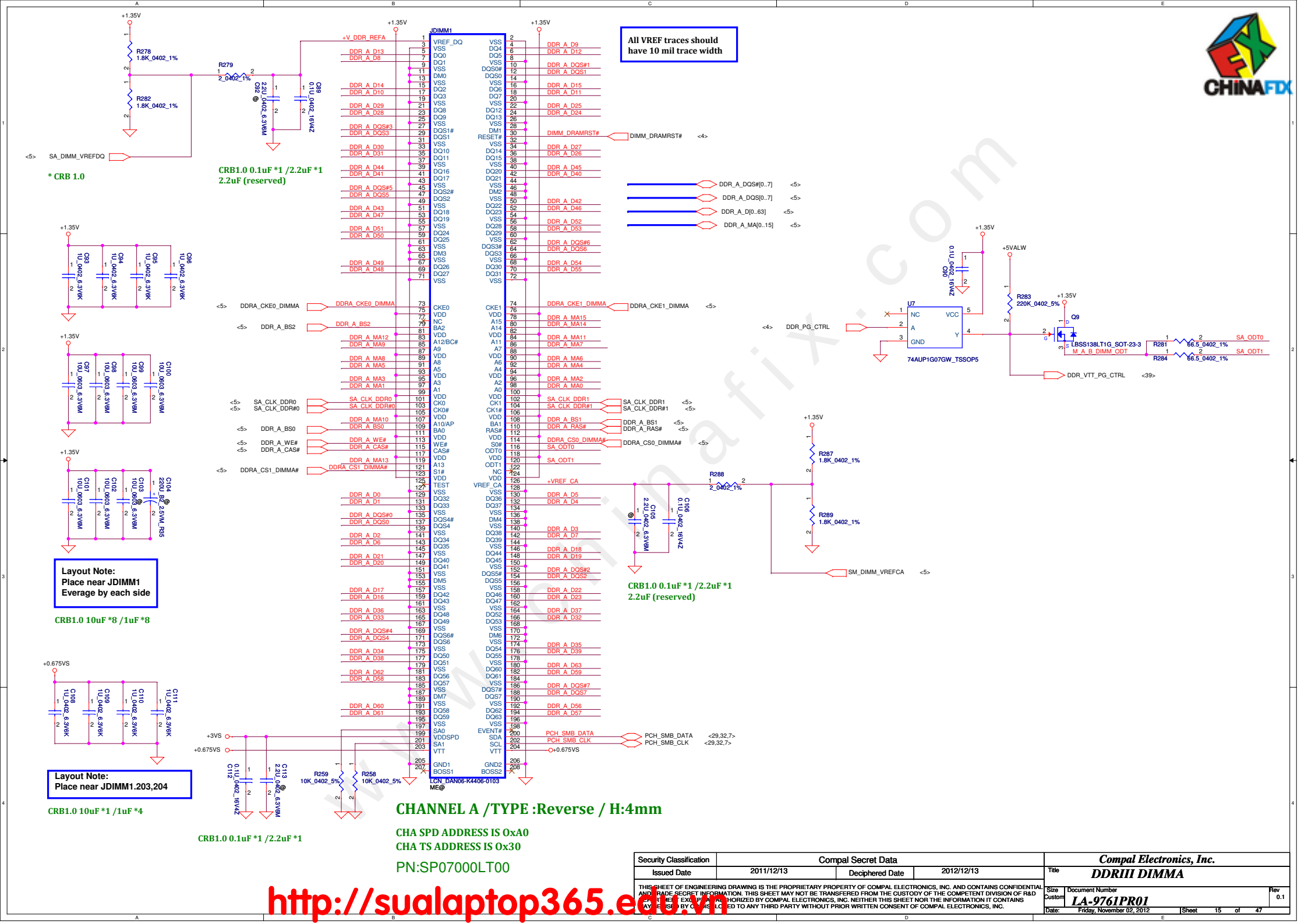

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Title: DDRIII DIMMA			
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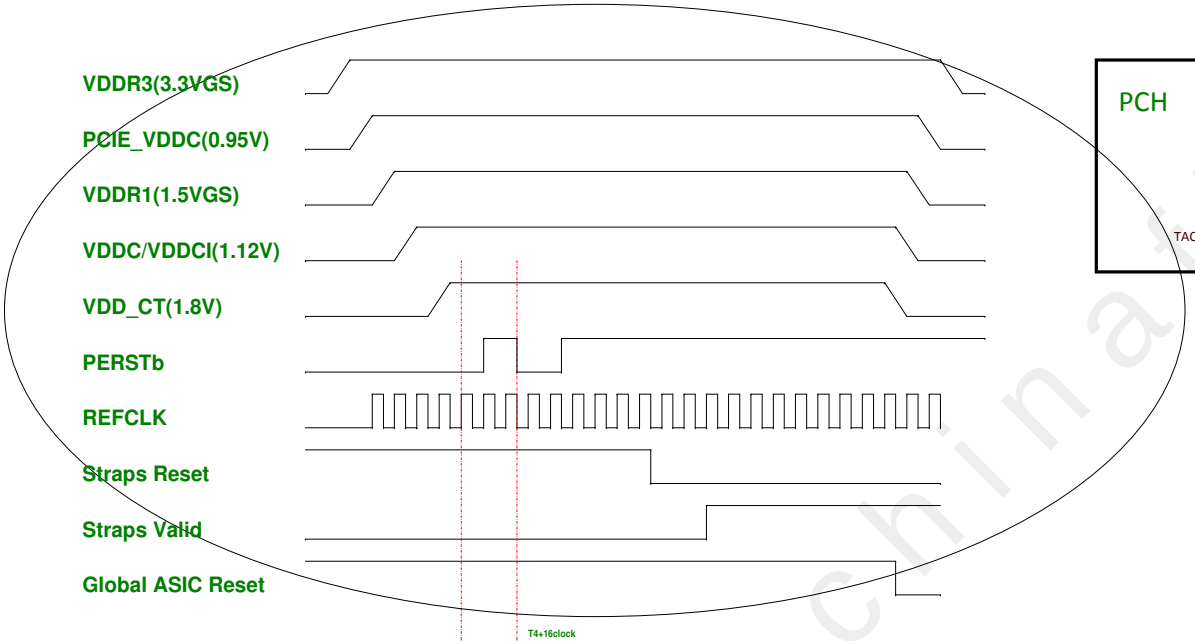
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

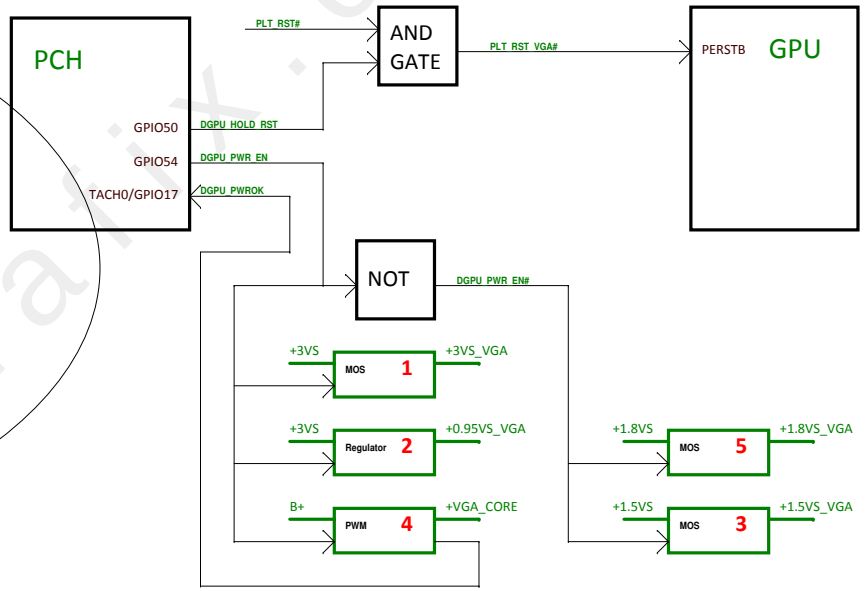
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



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Title: MARS_Note

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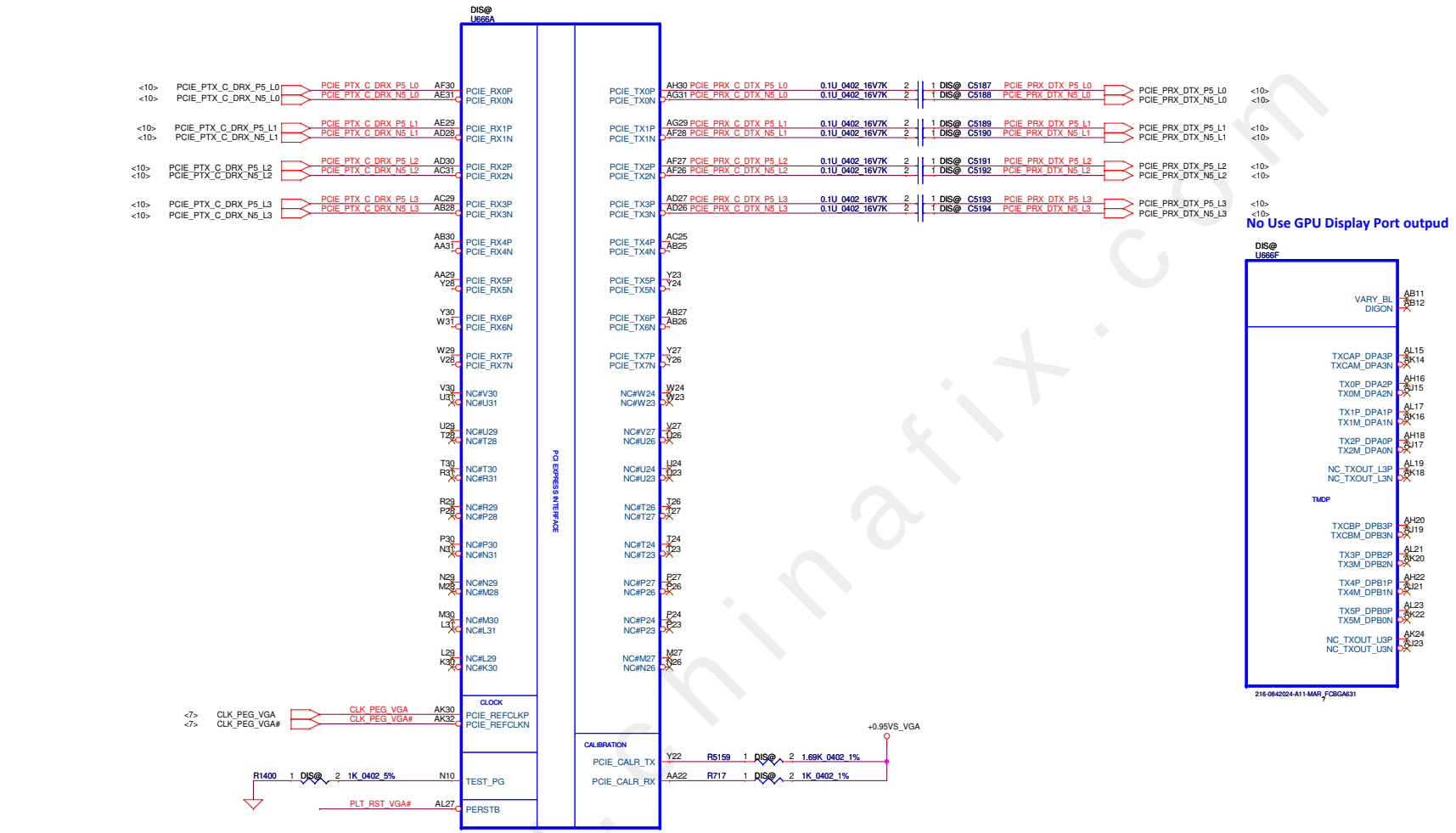

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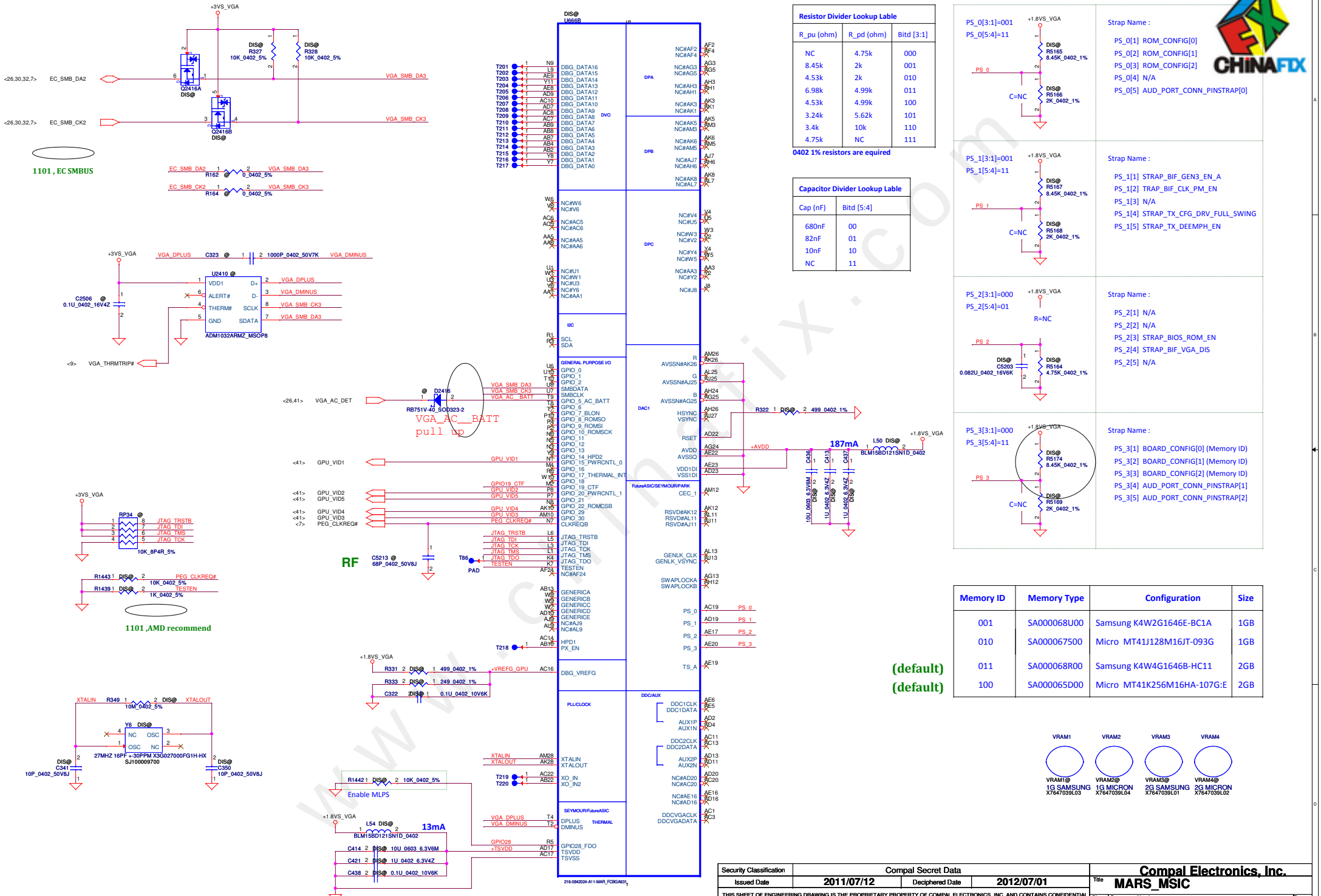

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Memory ID	Memory Type	Configuration	Size
001	SA000068U00	Samsung K4W2G1646E-BC1A	1GB
010	SA000067500	Micro MT41J128M16JT-093G	1GB
011	SA000068R00	Samsung K4W4G1646B-HC11	2GB
100	SA000065D00	Micro MT41K256M16HA-107G:E	2GB

(default)
(default)

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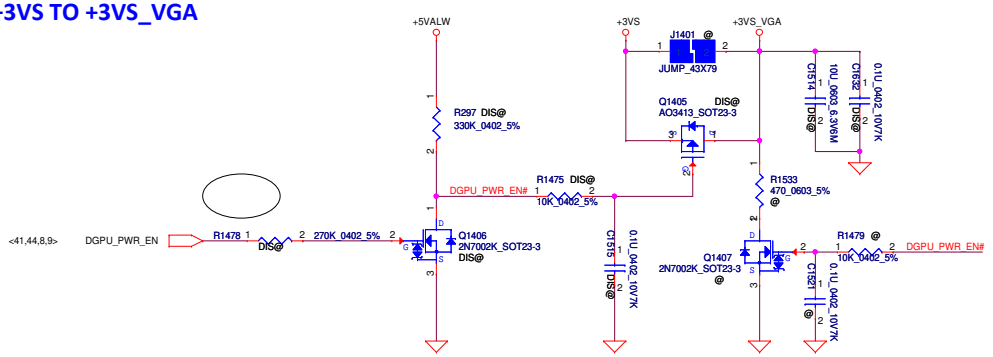
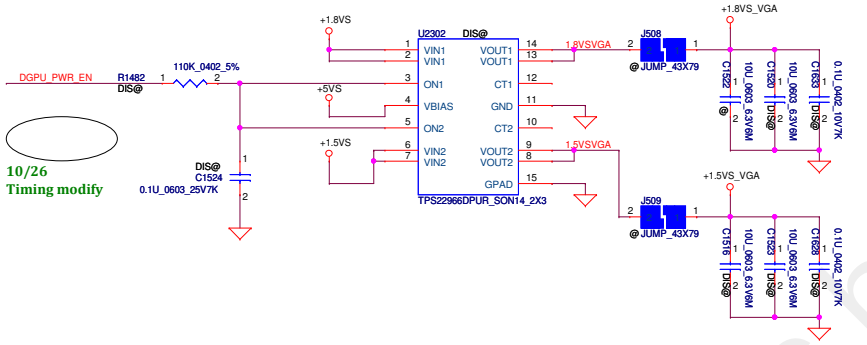
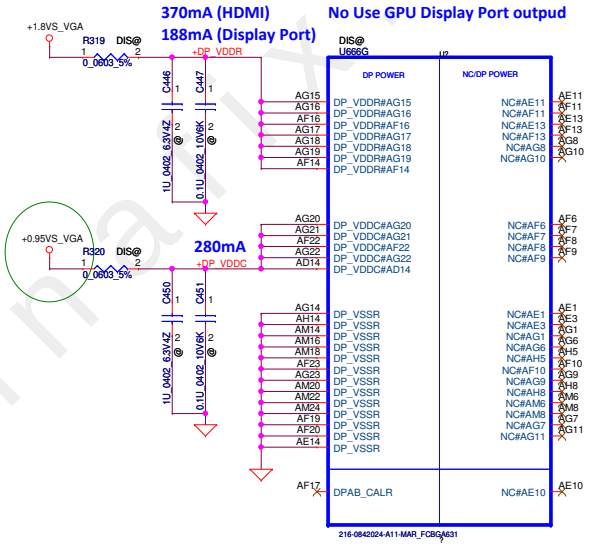
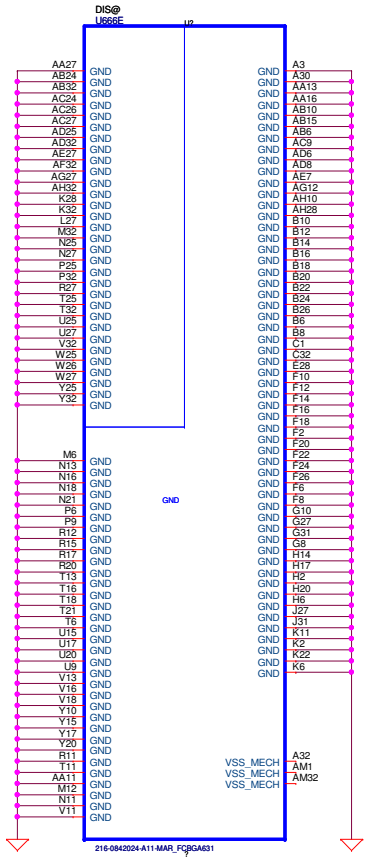
+3VS TO +3VS_VGA



+1.8VS TO +1.8VS_VGA
+1.5V TO +1.5VS_VGA







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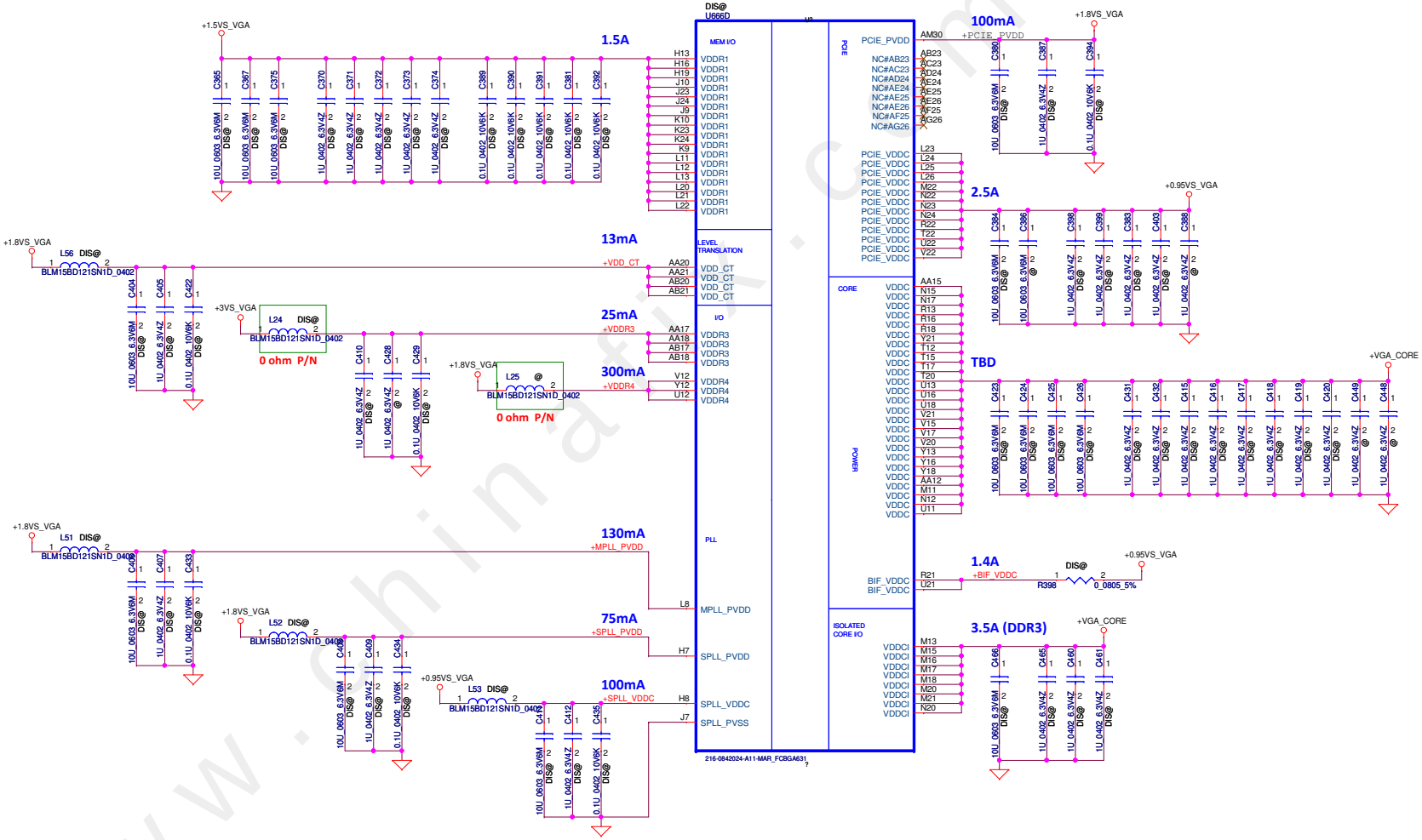
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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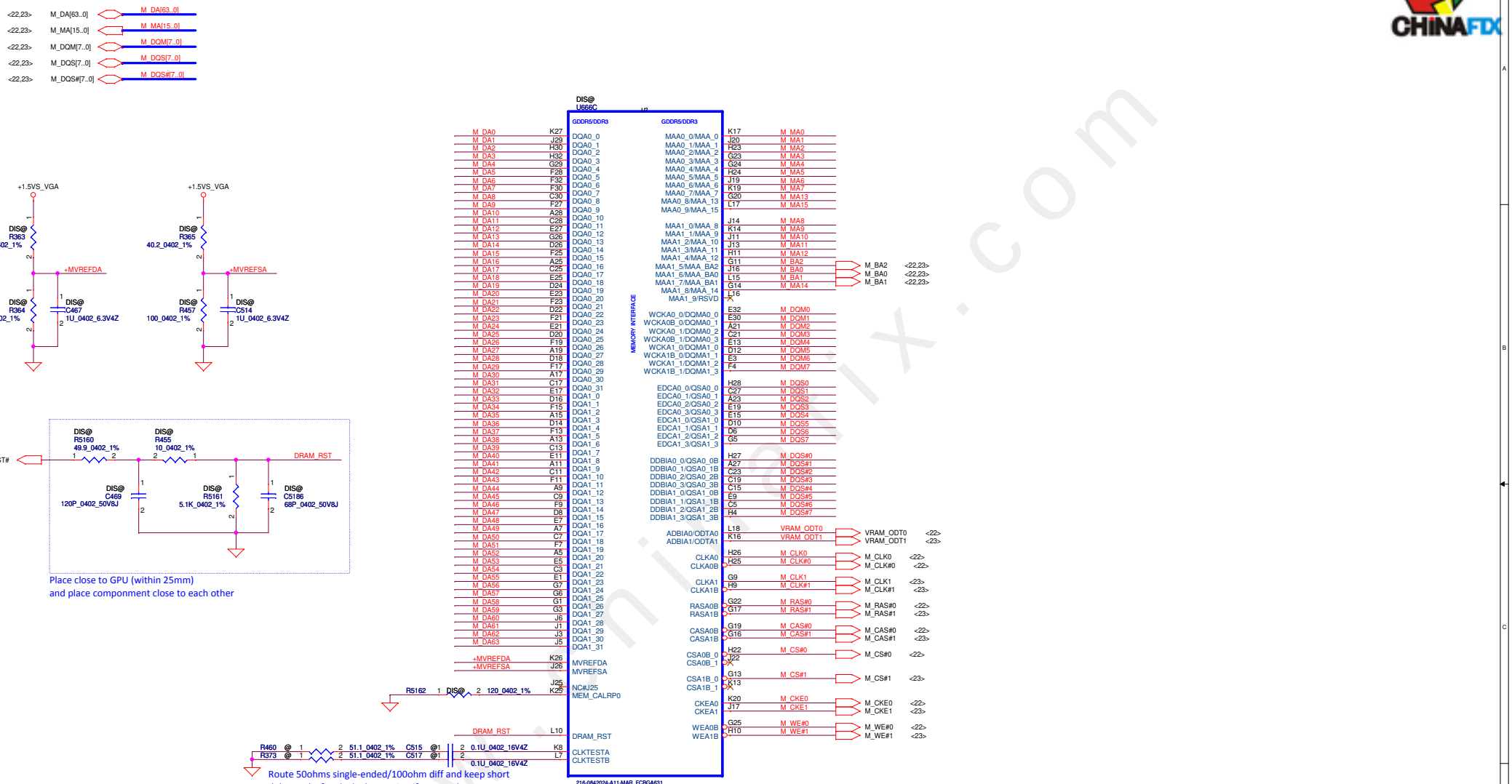

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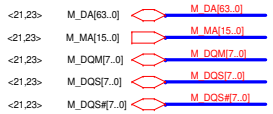
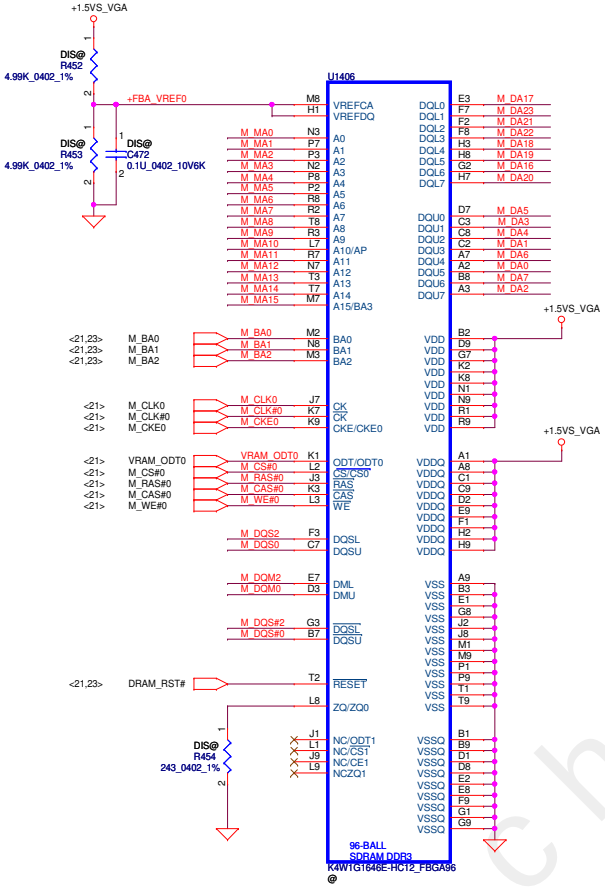
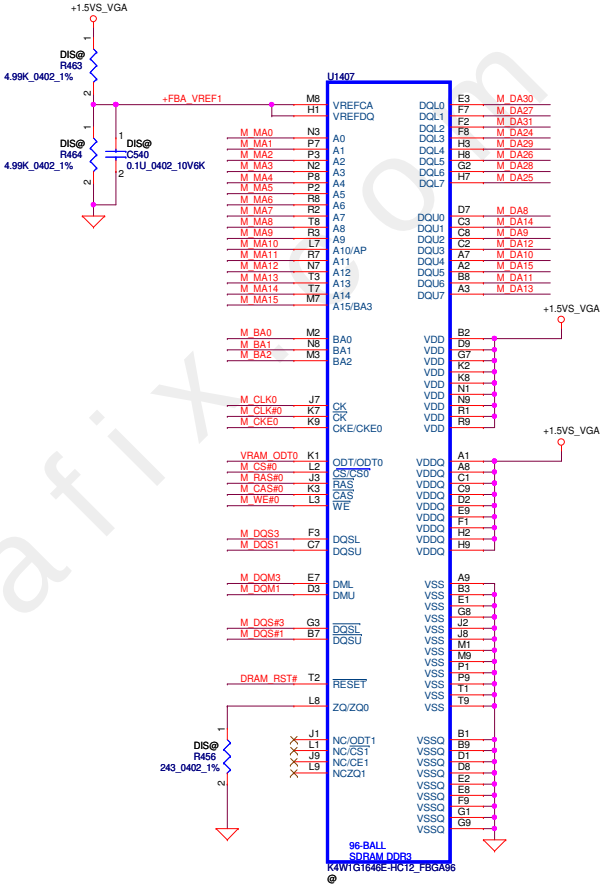
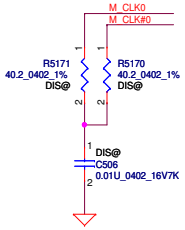
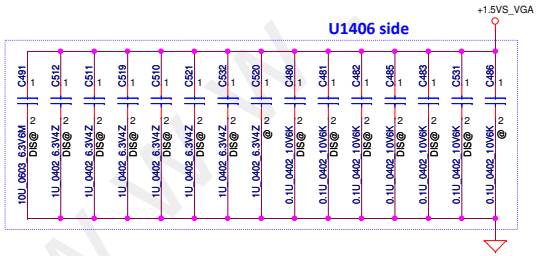
Memory Partition A - Lower 32 bits

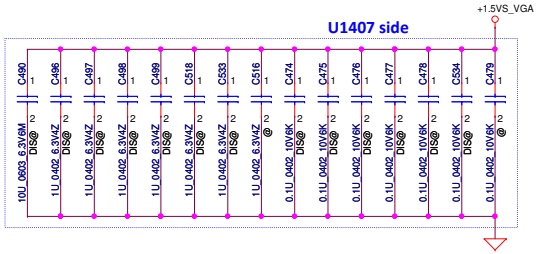












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Title	MARS_VRAM A Lower		
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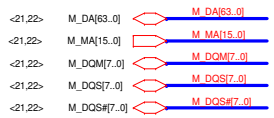
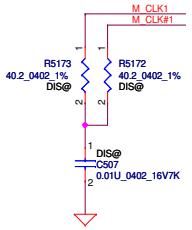
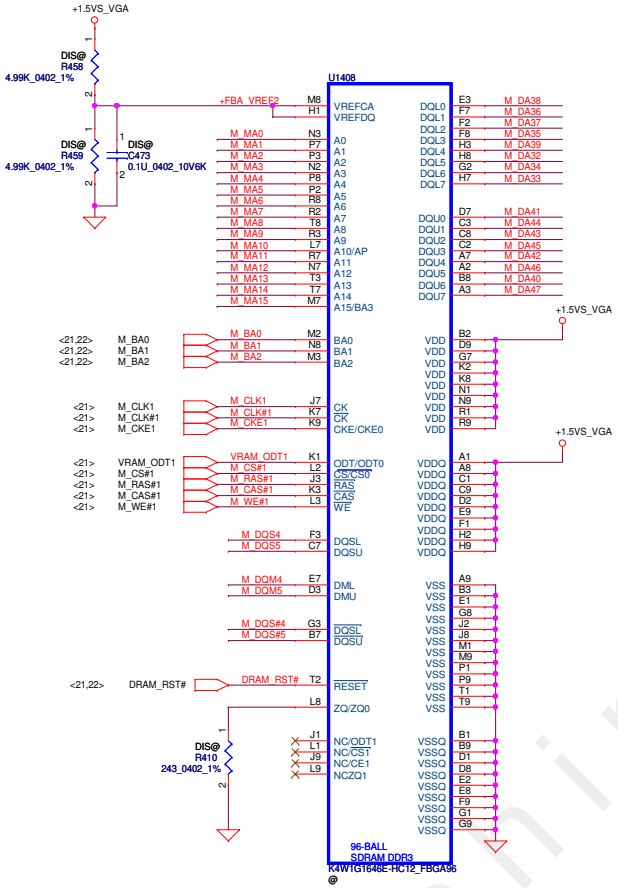
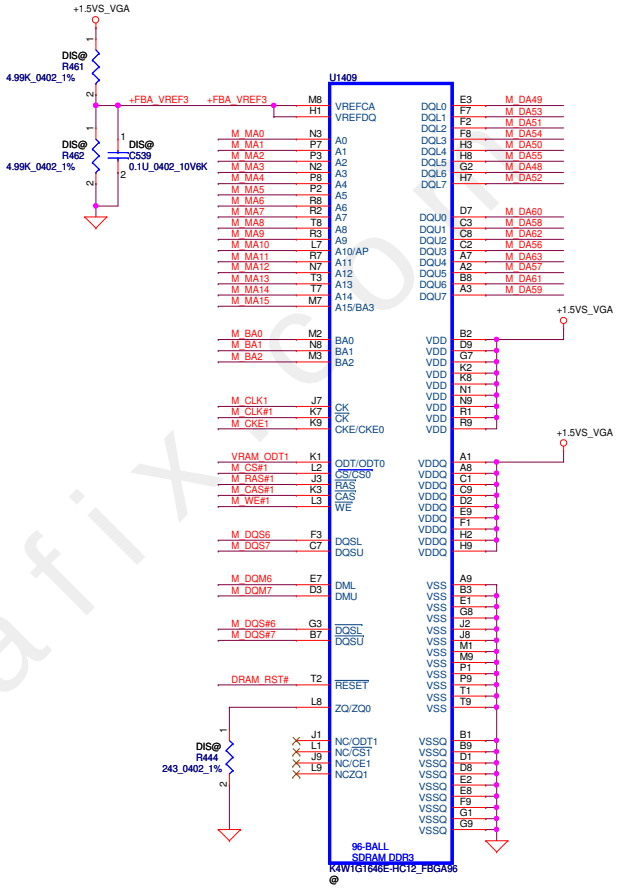
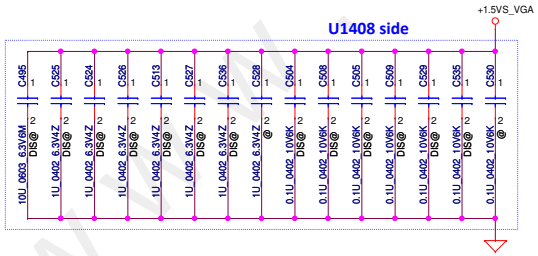
Memory Partition A – Upper 32 bits

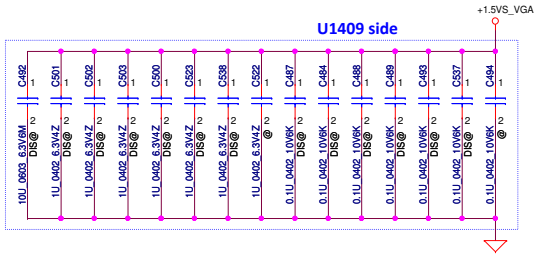












Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: MARS_VRAM A Upper

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 23 of 47

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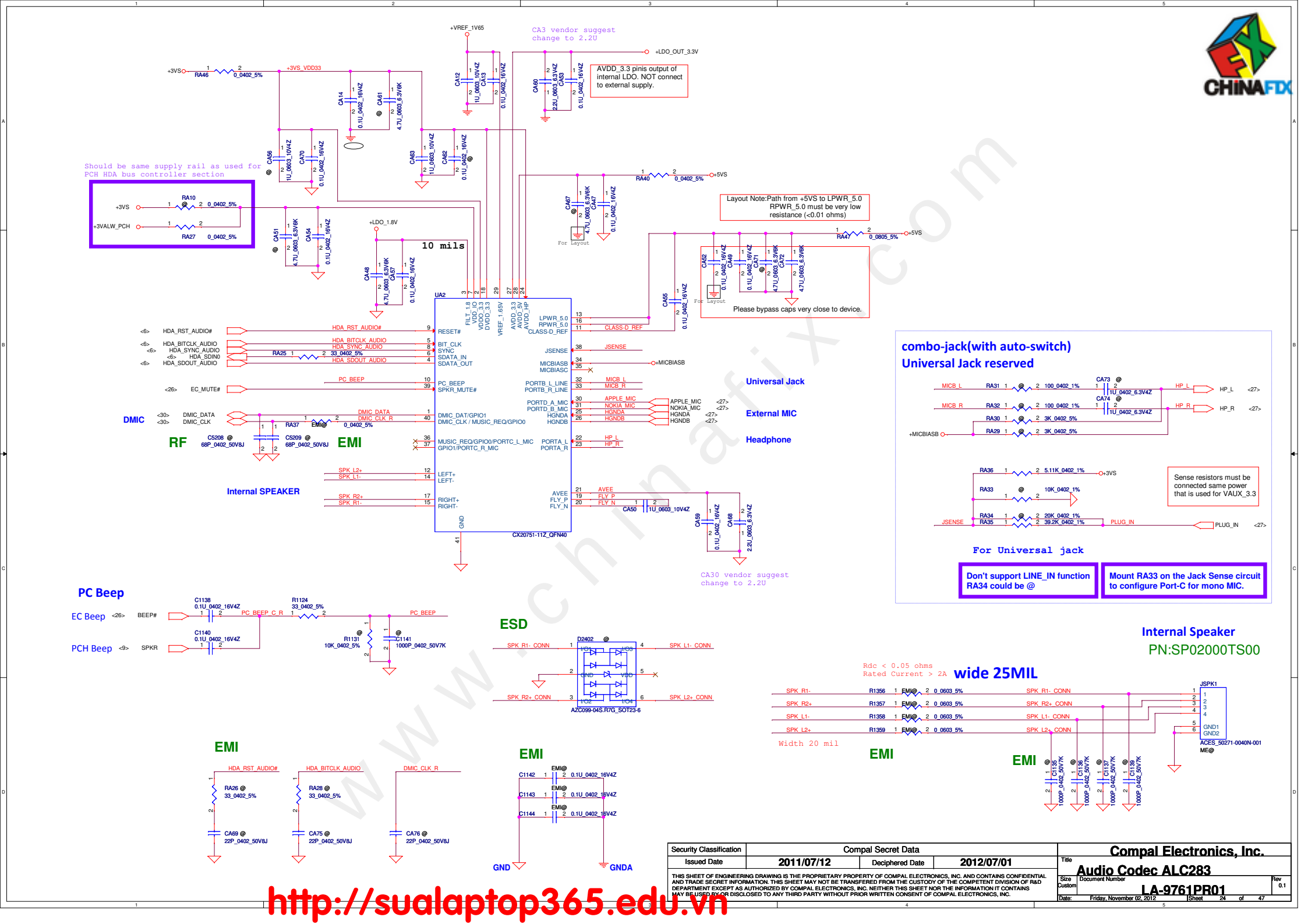

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: Audio Codec ALC283

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 24 of 47

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+3_LAN Rising time (10%~90%) >1mS and <100mS

+3VALW W=60mils J1203 @ JUMP_43X39 +3V_LAN 370mA

+3V_LAN R1243 1 2 0_0603_5% +LAN_VDDREG

C1195 SWR@ 4.7U_0603_6.3V6K

C1196 SWR@ 0.1U_0402_16V4Z

These caps close to U1201 : Pin 23

+3V_LAN

C1260 0.1U_0402_16V4Z

C1261 0.1U_0402_16V4Z

These caps close to U1201 : Pin 11,32

LDO@ R1240 1 2 0_0603_5%

+LAN_REGOUT W=60mils

L35 SWR@ 2.2UH +-5% NLC252018T-2R2J-N

W=60mils +LAN_VDD10

LDO@ C1251 0.1U_0402_16V4Z

C1185 SWR@ 4.7U_0603_6.3V6K

C1183 SWR@ 0.1U_0402_16V4Z

C1245 .1U@ 0402_16V7K

C1254 0.1U_0402_16V4Z

C1253 0.1U_0402_16V4Z

C1252 0.1U_0402_16V4Z

C1255 0.1U_0402_16V4Z

C1257 0.1U_0402_16V4Z

(Should be place within 200 mils)
These components close to U1201 : Pin 24

These components close to U1201 : Pin 3,8,22,30

1uF reserved on Pin 20

+3V_LAN

R2220 1 @ 2 10K_0402_5% LAN_WAKE#

R2222 1 @ 2 10K_0402_5% LAN_CLKREQ#

PU PCH side

C1239 15P_0402_50V8J XTLI_R

R1236 0_0402_5% XTLI

Y1201 25MHZ_12PF_7V25000012

GND GND

C1237 15P_0402_50V8J XTLO

8111F-VB support X'tal free

These caps close to U1201

LAN_MDI0+ LAN_MDI0- +LAN_VDD10 LAN_MDI1+ LAN_MDI1- LAN_MDI2+ LAN_MDI2- +LAN_VDD10 LAN_MDI3+ LAN_MDI3- +3V_LAN LAN_CLKREQ#

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N

HSOP HSON PERSTB ISOLATEB LANWAKEB DVDD10 VDDREG REGOUT LED2 LED1/GPIO LED0 CKXTAL1 CKXTAL2 AVDD10 RSET AVDD33 GND

PCIE_PRX_C_DTX_P2 C1244 1 2 .1U 0402 16V7K PCIE_PRX_DTX_P2

PCIE_PRX_C_DTX_N2 C1240 1 2 .1U_0402_16V7K PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB R1238 1 2 1K_0402_5%

LAN_WAKE# R1244 1 2 0_0402_5% +3VS

+LAN_VDD10 R1245 @ 2 0_0402_5%

VDDREG +LAN_REGOUT LANLINK_STATUS# LED2 LAN_ACTIVITY# XTLI +LAN_VDD10 LAN_RSET +3V_LAN

T60 @

R1235 1 2 2.49K_0402_1%

PCIE_PRX_DTX_P2 <10>
PCIE_PRX_DTX_N2 <10>
PLT_RST_BUF# <17,26,29,30,7,8>

EC_PME# <26>
PCH_PCIE_WAKE# <8,9>

<7> LAN_CLKREQ#
<10> PCIE_PTX_C_DRX_P2
<10> PCIE_PTX_C_DRX_N2
<7> CLK_PCIE_LAN
<7> CLK_PCIE_LAN#

U9 RTL8111GS-CG_QFN32_4X4

ISOLATEB R1242 15K_0402_5%

A2 A1 1 2 3 4 5 6 7 8 B2 B1

NEW(referDC234005L00鍍黑鎳)
MB TO TOP 4.95 move up 1.35)

NEW(refer 130452-D鍍黑鎳)
MB TO TOP 4.95 move up 1.35)

+V_DAC C1288 0.01U_0402_16V7K

TS1202 350UH_IH-160

TCT1 TD1+ TD1- TCT2 TD2- TD2+ TCT3 TD3- TD3+ TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2- MX2+ MCT3 MX3+ MX3- MCT4 MX4+ MX4-

LAN_MDI0- LAN_MDI0+ LAN_MDI1- LAN_MDI1+ LAN_MDI2+ LAN_MDI2- LAN_MDI3+ LAN_MDI3-

RJ45_MDO0- RJ45_MDO0+ RJ45_MDO1- RJ45_MDO1+ RJ45_MDO2+ RJ45_MDO2- RJ45_MDO3+ RJ45_MDO3-

R1260 75_0402_5% RJ45_GND

R1259 75_0402_5%

R1257 75_0402_5%

R1258 75_0402_5%

C1289 EMI@ 10P_1206_2KV8J

EMI

EMI

D1209 @ MCT1 LSE-200NX3216TRLF_1206-2

D1210 @ MCT2 LSE-200NX3216TRLF_1206-2

D1211 @ MCT3 LSE-200NX3216TRLF_1206-2

D1212 @ MCT4 LSE-200NX3216TRLF_1206-2

ESD

D1207 ESD@ LAN_MDI0- LAN_MDI1+ LAN_MDI0+ LAN_MDI1-

D1208 ESD@ LAN_MDI2- LAN_MDI3+ LAN_MDI2+ LAN_MDI3-

I/O4 I/O2 VDD GND I/O3 I/O1 AZC099-04S.R7G_SOT23-6

PN:DC234005L00

RJ-45 Conn.

LANLINK_STATUS# R1246 510_0402_5% @ C1265 220P_0402_50V7K

LAN_ACTIVITY# R1241 510_0402_5% @ C1270 220P_0402_50V7K

+3V_LAN +3V_LAN

LANLED_LINK# LANLED_ACT#

JRJ45 SANTA_130452-D ME@

Green LED- Green LED+ Yellow LED- Yellow LED+

RJ45_MDO0+ RJ45_MDO0- RJ45_MDO1+ RJ45_MDO2+ RJ45_MDO2- RJ45_MDO1- RJ45_MDO3+ RJ45_MDO3-

PR1+ PR1- PR2+ PR3+ PR3- PR2- PR4+ PR4- G2 G1

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: LAN RTL8111GS

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 25 of 47

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Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30

10/26 PWR

If +3VS leakage on S3 mode please check EC_MUTE#

BOTTOM SIDE

SN111005800 by ME drawing

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 26 of 47

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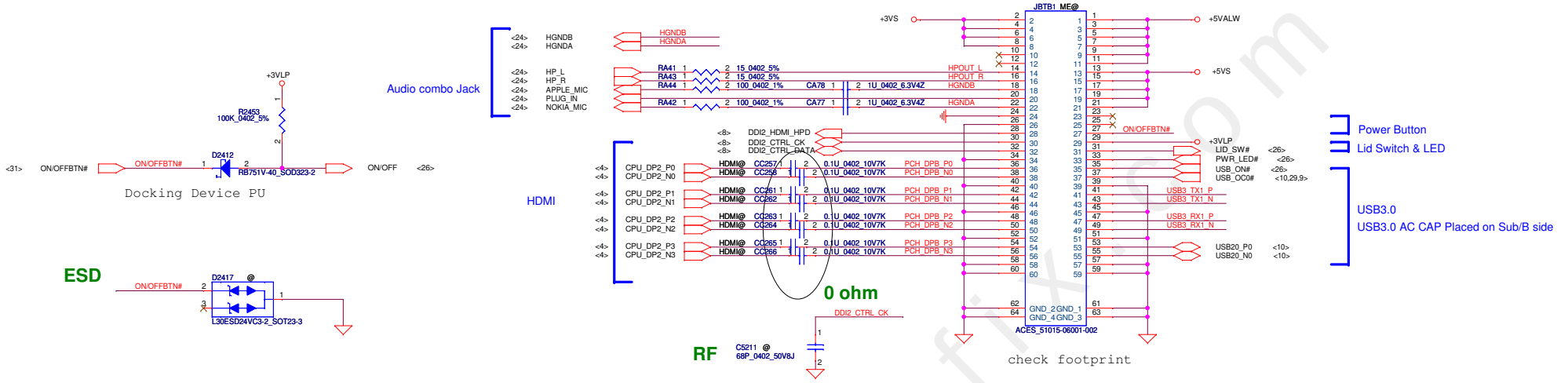
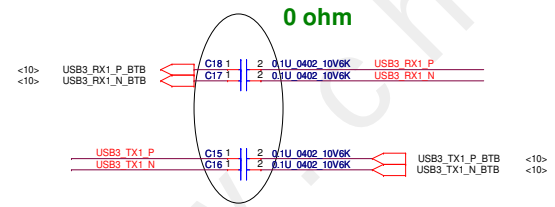
I/O Board CONN.

PN:LTCX004C100

Connector: 0.3A / pin



USB 3.0 ReDriver



USB 3.0 ReDriver change to Sub/B

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.			
Title: PBTN/FAN/TPM/RTC/IO Board			
Size: Custom	Document Number: LA-9761PR01		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 27 of 47		

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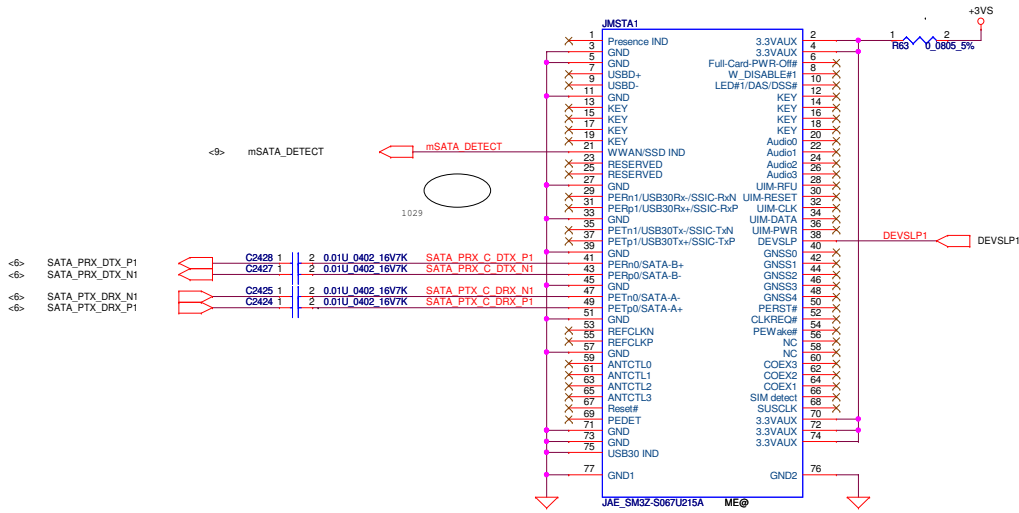
mSATA CONN.

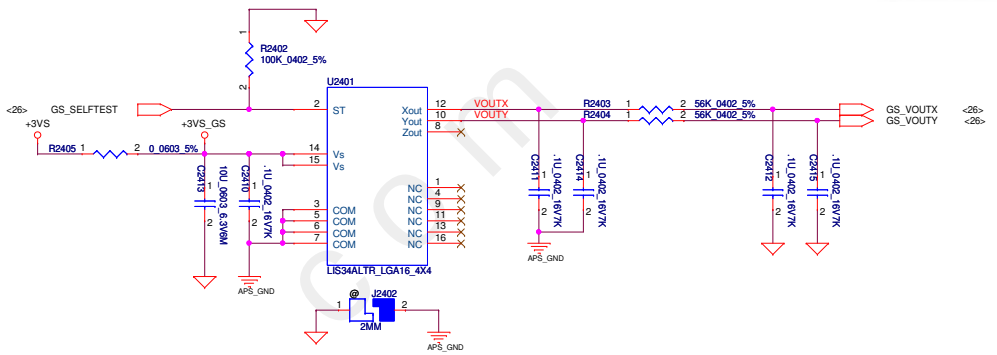
PN:??

LTCX004IO00



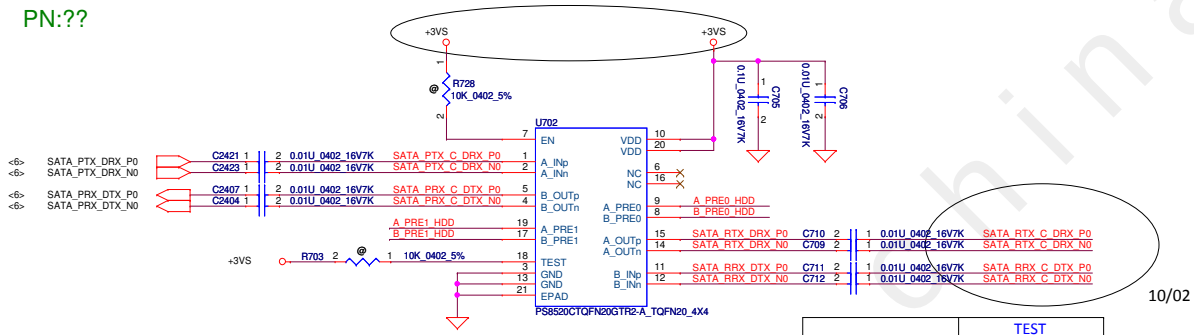
APS G-Sensor

PN:??



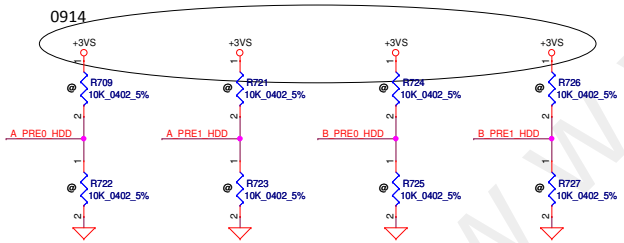
SATA ReDriver

PN:??



10/02

0914



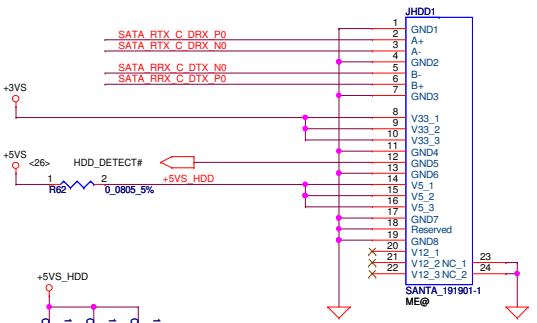
	TEST (Internal pull Low)
Normal operation (default)	Low
Compliance testing mode enable	High

	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High

SATA HDD CONN.

DEVSLP is not supported on legacy SATA connectors -502636 PDG1.0

PN:??



Close to conn

Pin 18 to GND for Gen 3

Pin 18 detect pin for SSD HDD

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Compal Electronics, Inc.

Title: HDD/mSATA/G-Sensor

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 28 of 47

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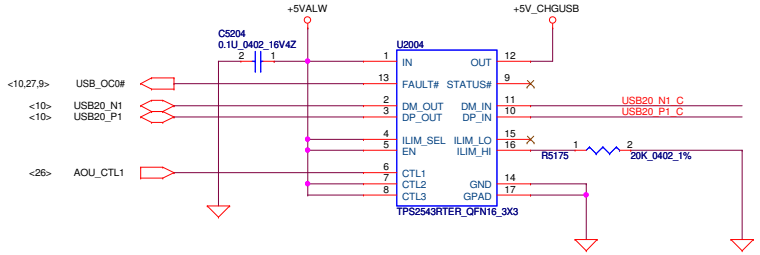
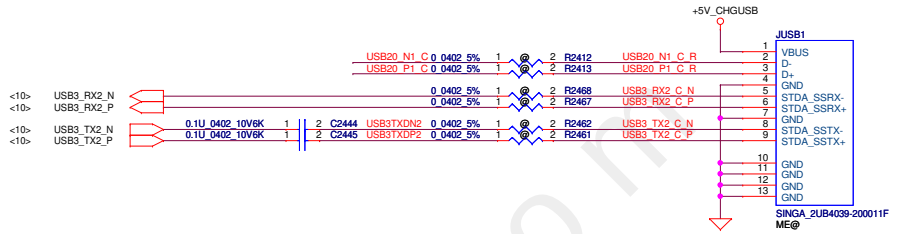
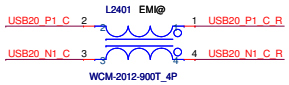
USB 3.0 Charger & Conn.

PN:LTCX004INB0

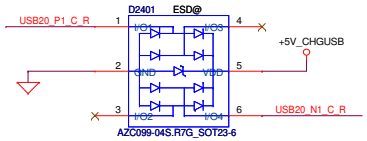




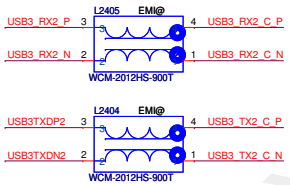
ESD



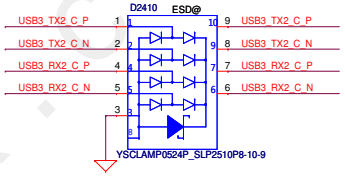
EMI



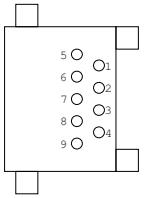
EMI



ESD



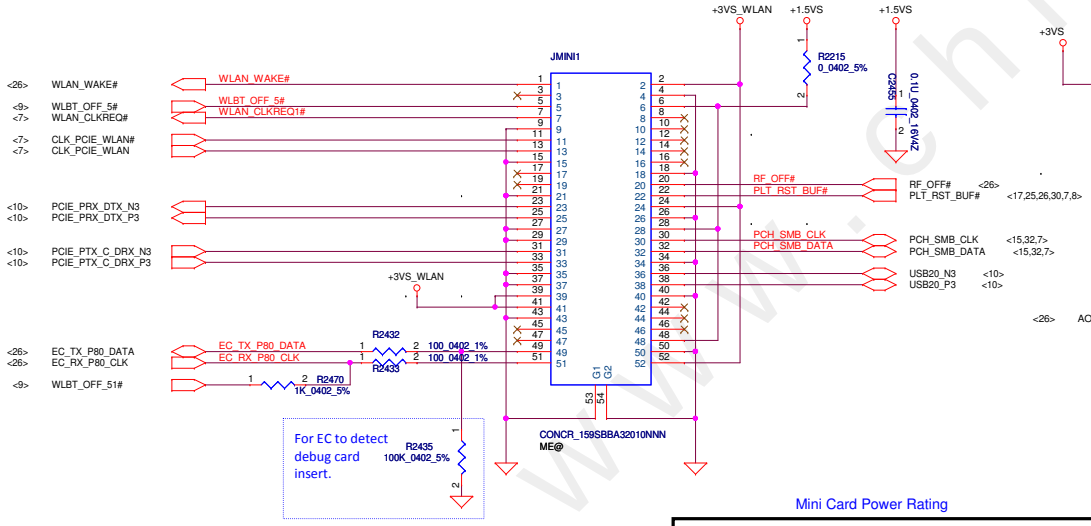
PIN1 VBUS
PIN2 D-
PIN3 D+
PIN4 GND
PIN5 RX-
PIN6 RX+
PIN7 GND
PIN8 TX-
PIN9 TX+

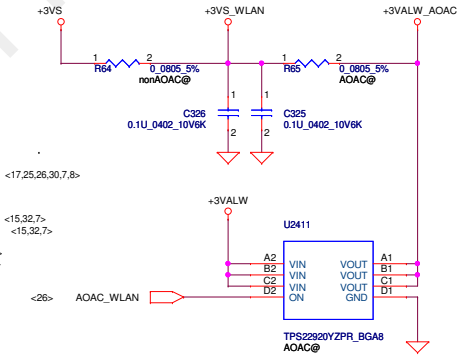


Mini-Express Card for WLAN/WiMAX(Half)

PN:LTCX004IR00

Need check WLAN/BT module OFF pin





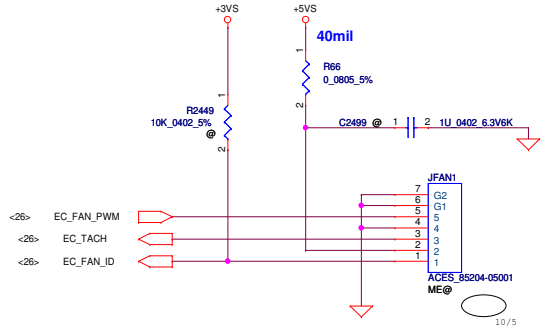
Controlled slew- rate to avoid inrush current

Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

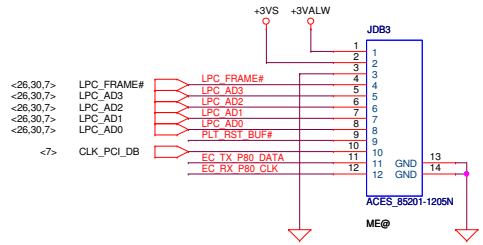
FAN CONN.

PN:??



Debug Conn.

PN:??



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Compal Electronics, Inc.

Title: USB 3.0 Connector & WLAN

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 29 of 47

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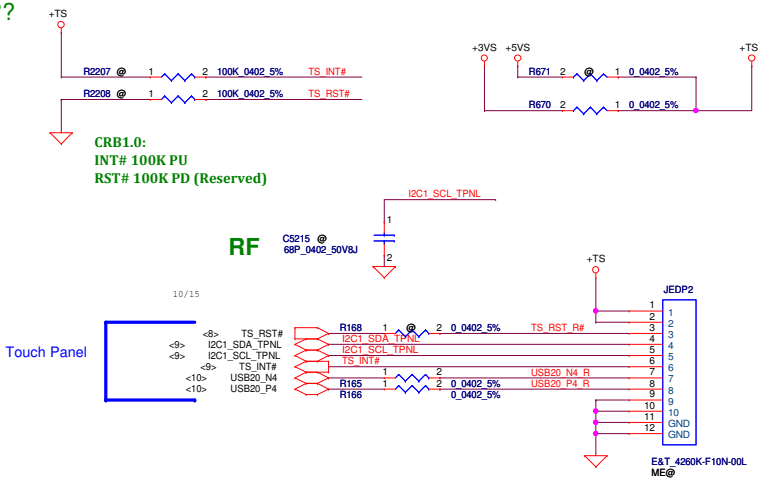
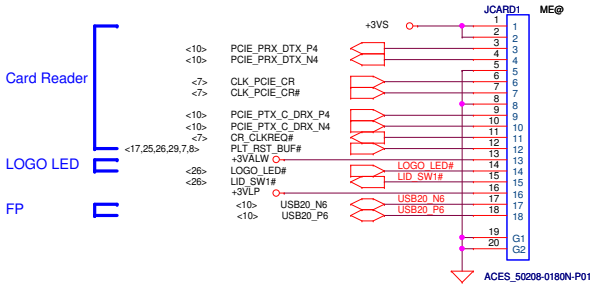
TOCUCH SCREEN CONN.

PN:??



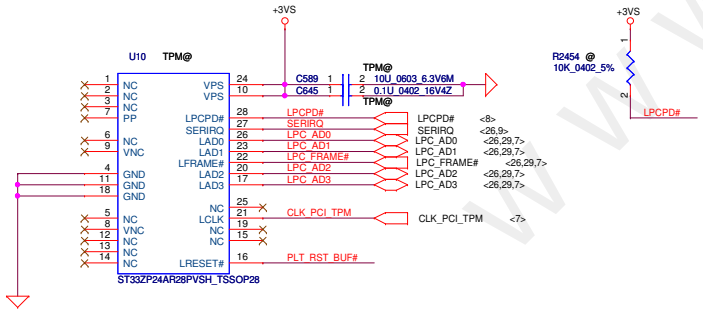
Card Reader CONN.

PN:??



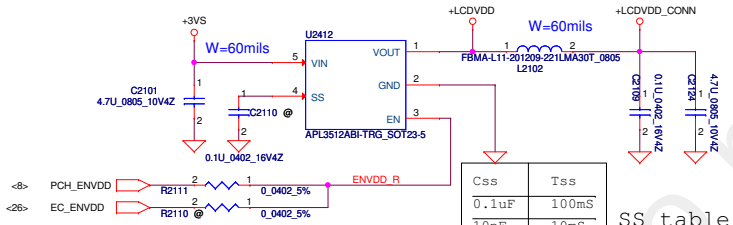
TPM

PN:??



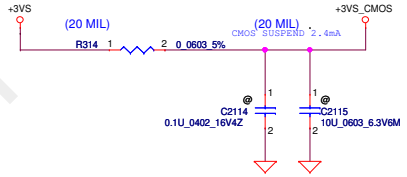
LCD PANEL Conn.

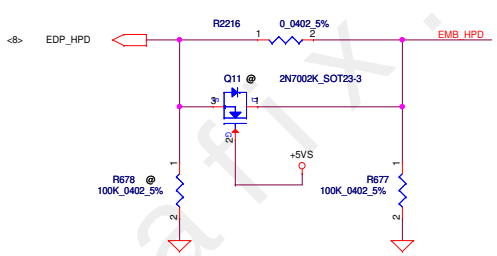
PN:??

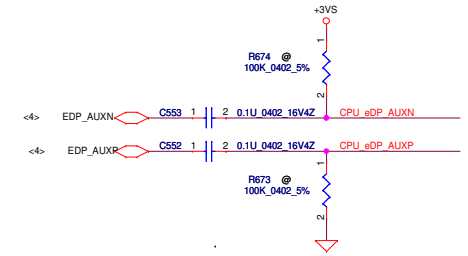


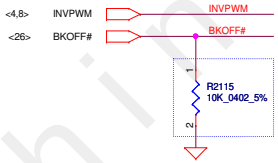
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

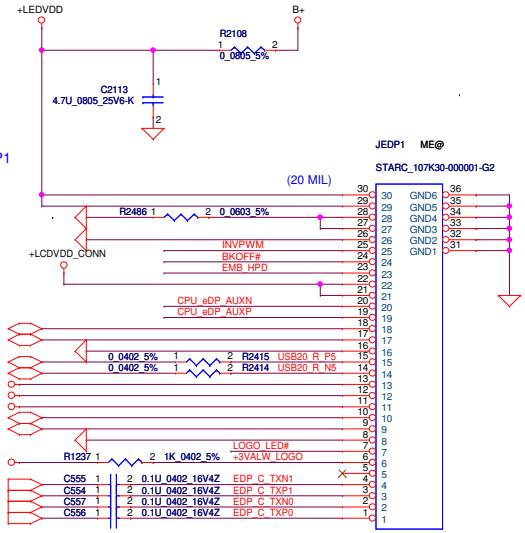
SS table

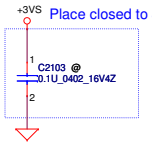


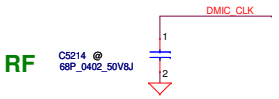


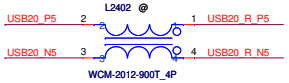


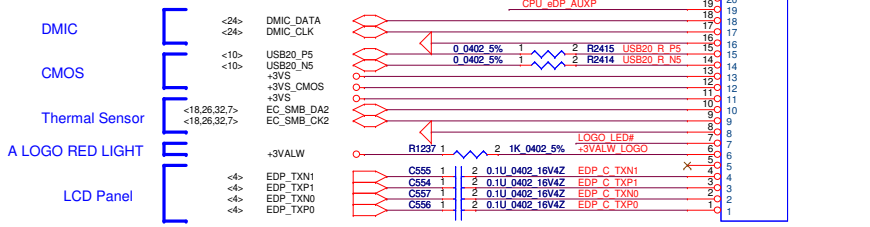












Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 30 of 47

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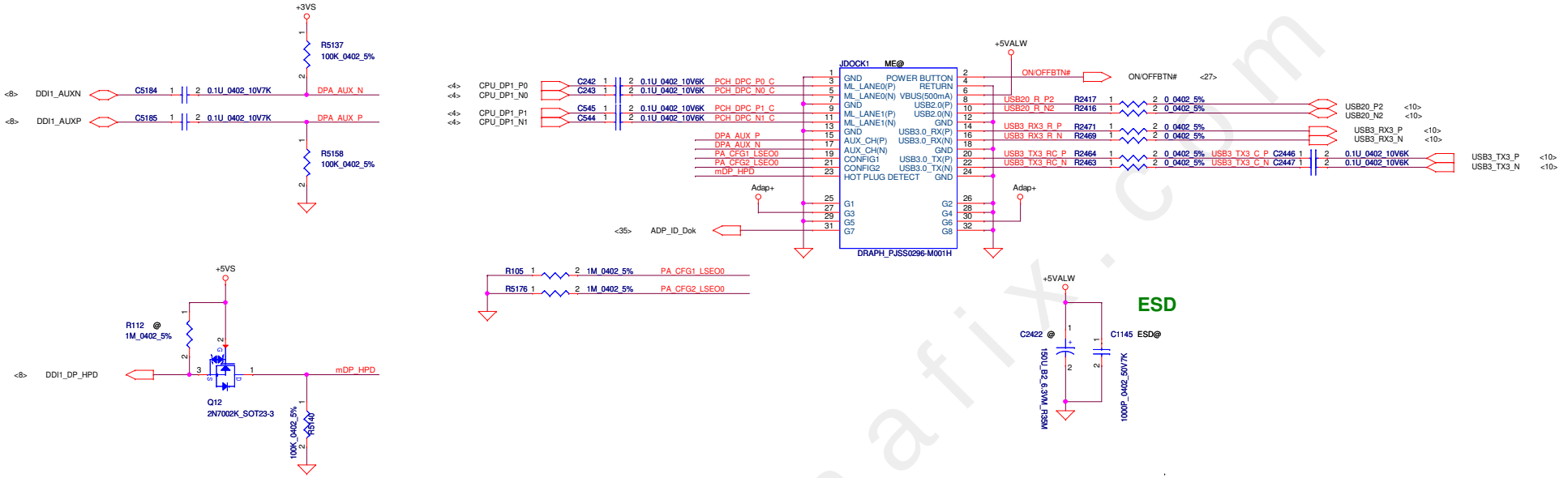
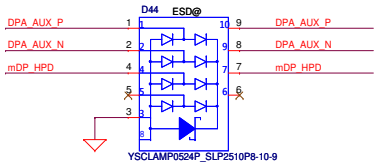
Docking Connector

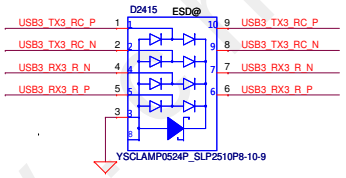
PN:??



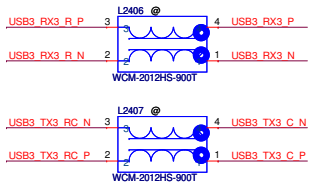
ESD



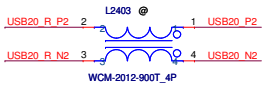
ESD

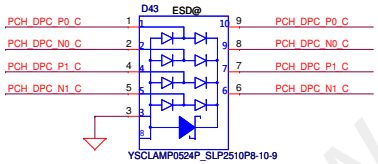


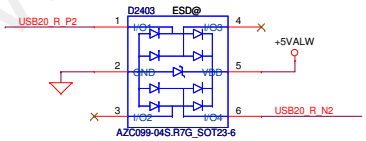
EMI



EMI







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: Docking

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 31 of 47

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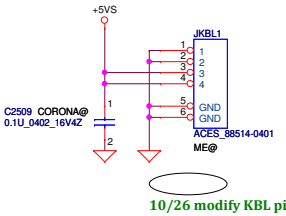
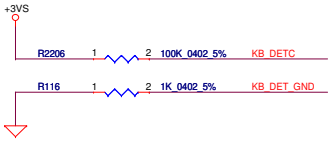
KB LIGHT CONN

PN:??

CORONA :JKB1+JKBL1
LABATT:JKB2



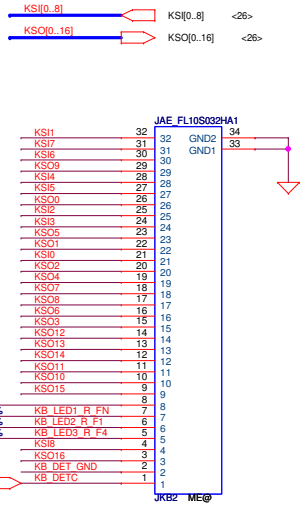
10/26 modify KBL pin define



KB_LED1 for Fn
KB_LED2 for F1
KB_LED3 for F4
Fn (S9)
D17 (GND)

INT_KBD Conn.

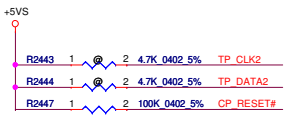
PN:??



10/26
LED seriel resistor

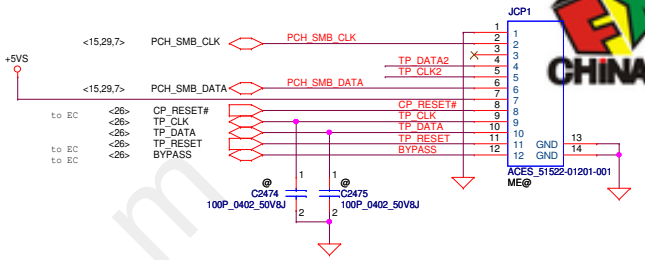
CLICK PAD CONN

PN:??



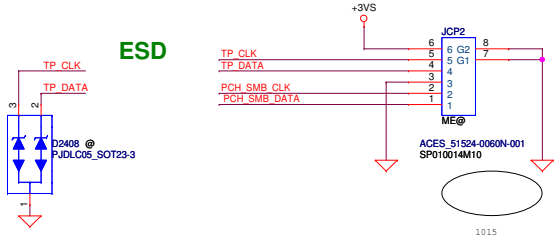
CORONA :JCP2
LABATT:JTP1+JCP1

(Labatt only)

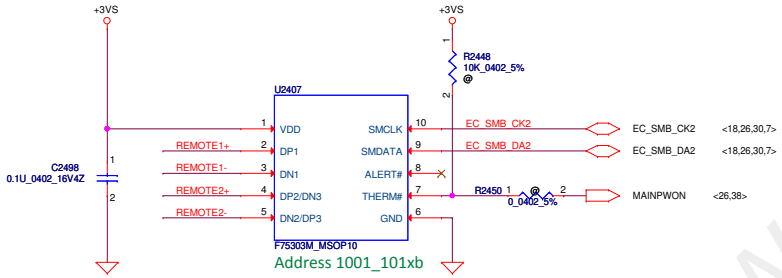


(Corona only)

ESD

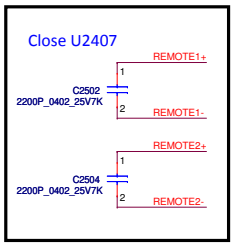


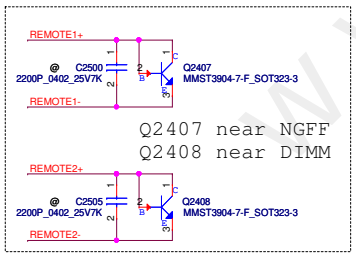
Fintek thermal sensor placed near CPU Core



Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR



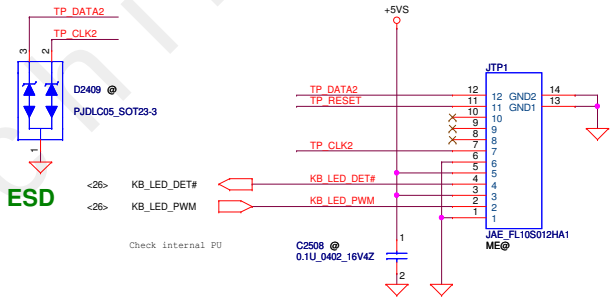


Q2407 near NGFF
Q2408 near DIMM

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

TRACK POINT CONN (Labatt only)

PN:??

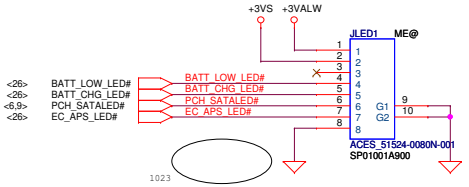


ESD

Check internal PU

LED Conn

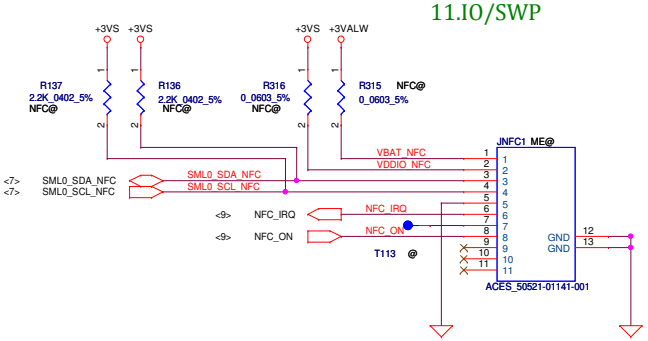
PN:??



NFC Conn

PN:??

Module Pin define
1.IP/VBAT
2.IP/VDDIO
3.IO/I2C-SDA
4.I/I2C-SCL
5.G/GND
6.O/IRQ-NFC
7.O/NFC_Presence#
8.I/REG_UP
9.OP/VDD_Ext_SE
10.IP/UIM_PWR
11.IO/SWP



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Compal Electronics, Inc.

Title: KB/CP/TP/FP/Thermal Sensor

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 32 of 47

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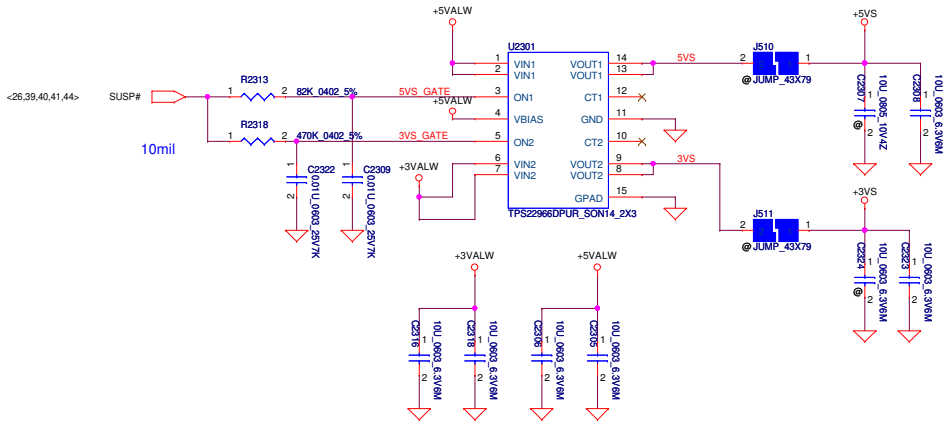
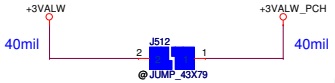
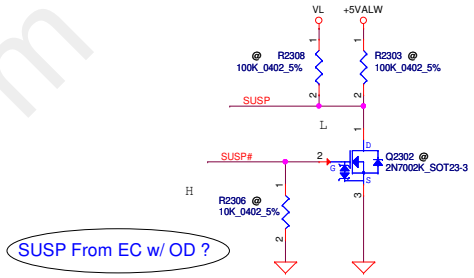
+5VALW TO +5VS
+3VALW TO +3VS



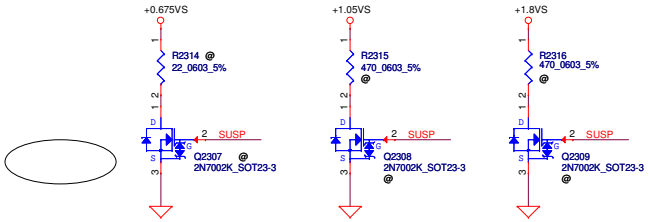
+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3





SUSP From EC w/ OD ?



10/26
1.SharkBay no need use discharge for S3 reduction
2.+0.675v support discharge circuit

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 33 of 47

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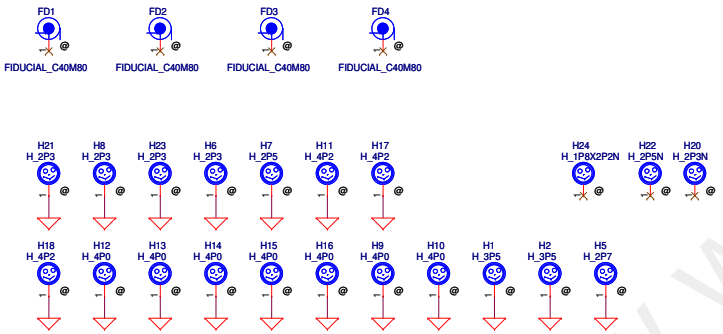
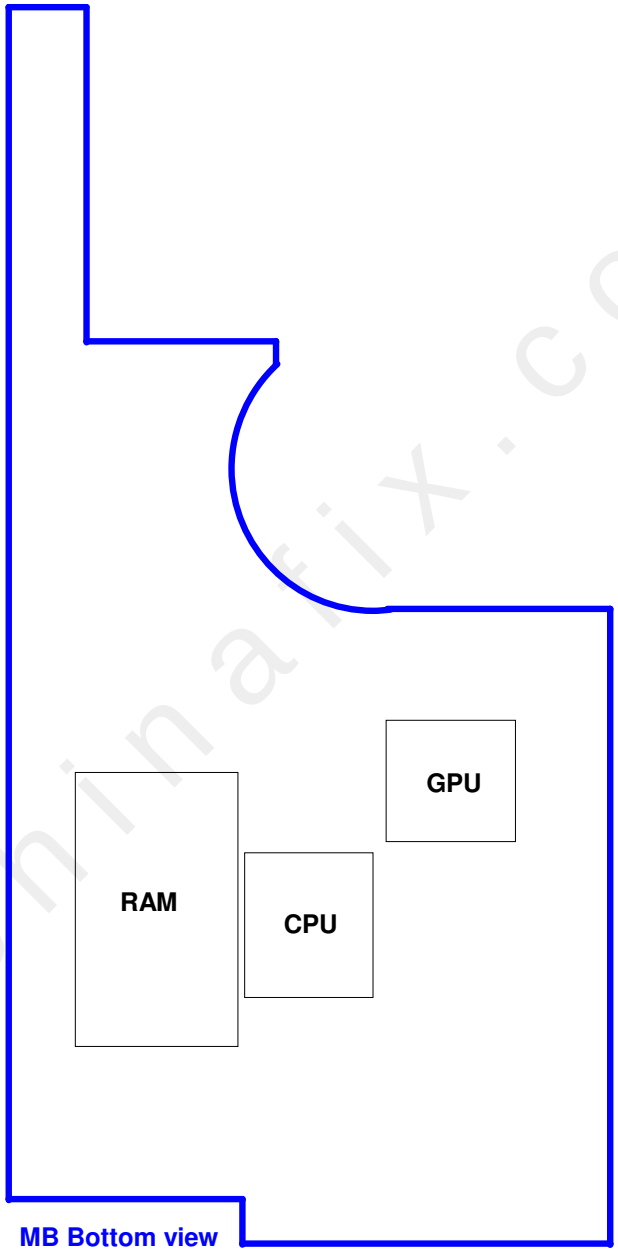
http://sualaptop365.edu.vn





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Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: Screw Hole

Size: Custom | Document Number: LA-9761PR01 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 34 of 47

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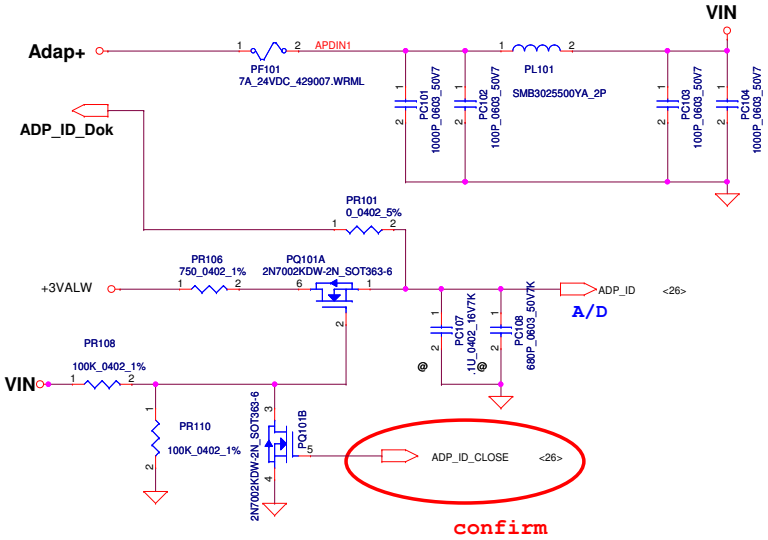
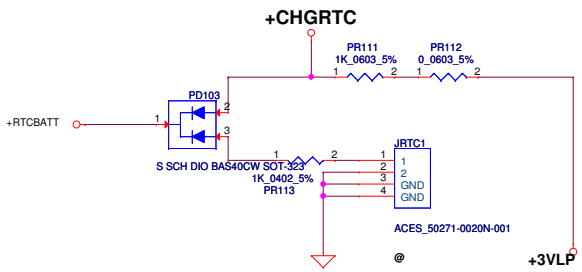
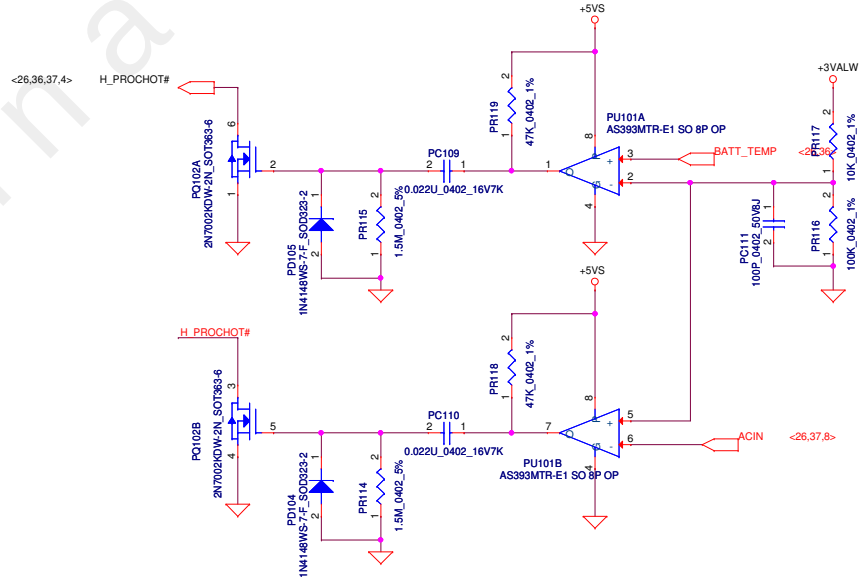


ADP_ID

AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection -Voltage(V)	<=0.663, >0.234	<=1.134, >0.693	<=1.618 >1.172





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Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR DCIN

Size: Custom | Document Number: VIUS1 | Rev: 0.4

Date: Friday, November 02, 2012 | Sheet 35 of 47

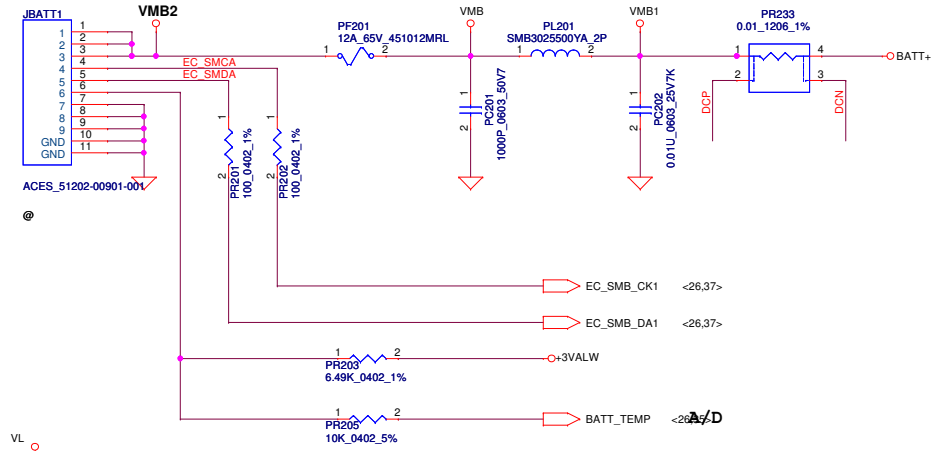
http://sualaptop365.edu.vn

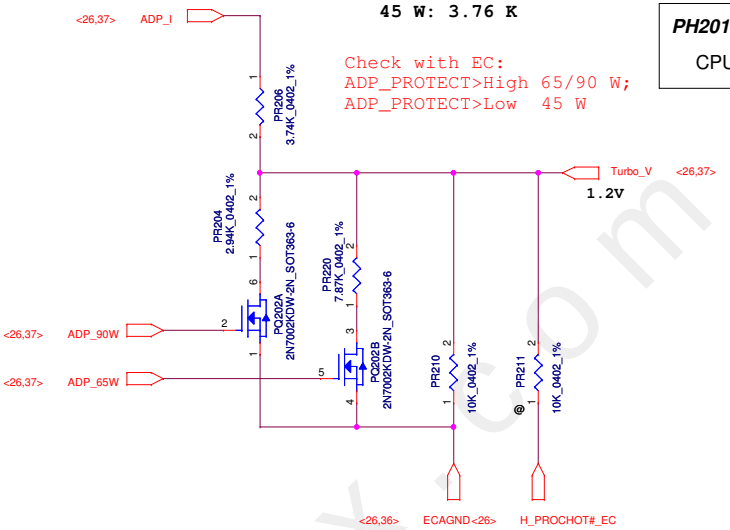
65/90 W: 8.66 K
45 W: 3.76 K

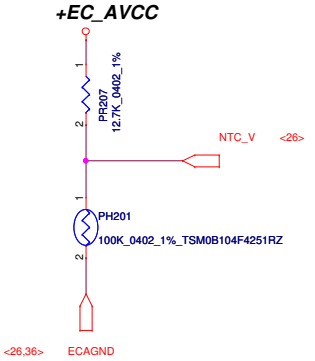
Check with EC:
ADP_PROTECT>High 65/90 W;
ADP_PROTECT>Low 45 W

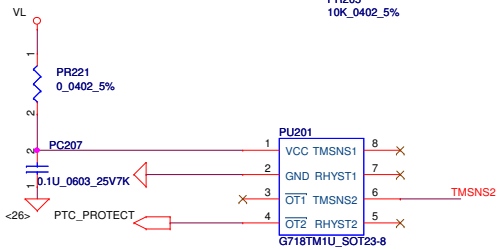
PH201 under CPU botten side :

CPU thermal protection at 93 degree C





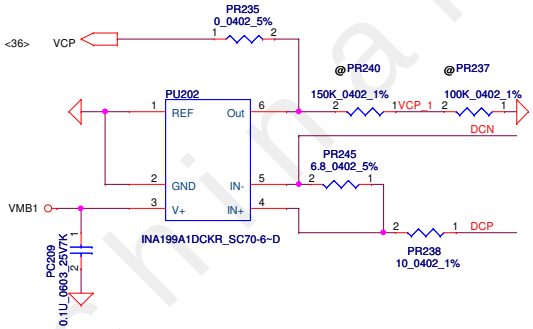


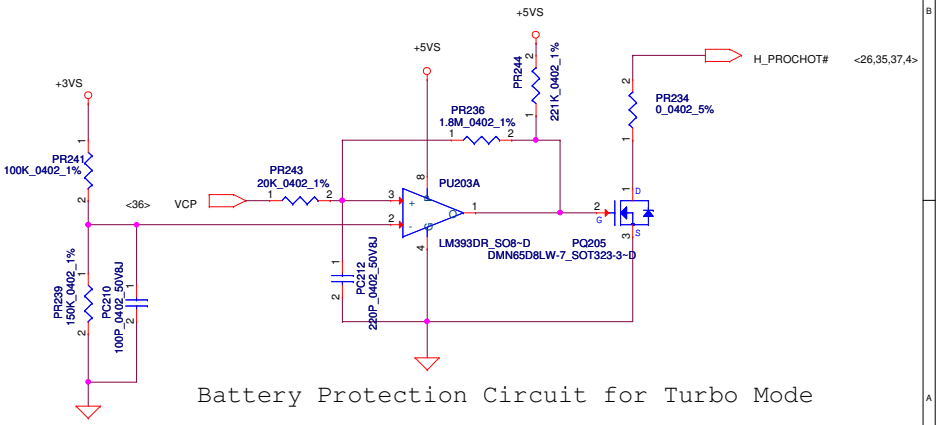


A/D

PH201: Temp. Rman. Rnor. Rmin. (Kohm)

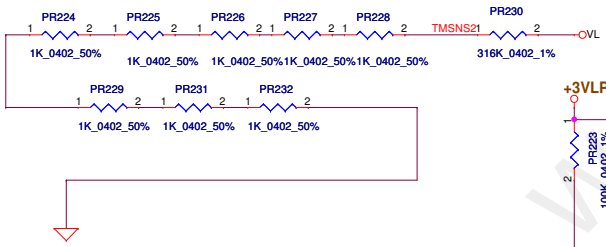
93 7.3419 7.0792 6.8253

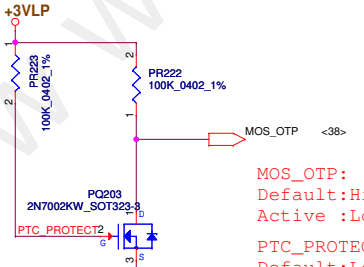




Battery Protection Circuit for Turbo Mode

Posestor





MOS_OTP:
Default:High
Active :Low

PTC_PROTECT:
Default:Low

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.			
Title: PWR-BATTERY CONN/OTP			
Size: Custom	Document Number: VIUS1		Rev: 0.4
Date: Friday, November 02, 2012	Sheet 36 of 47		

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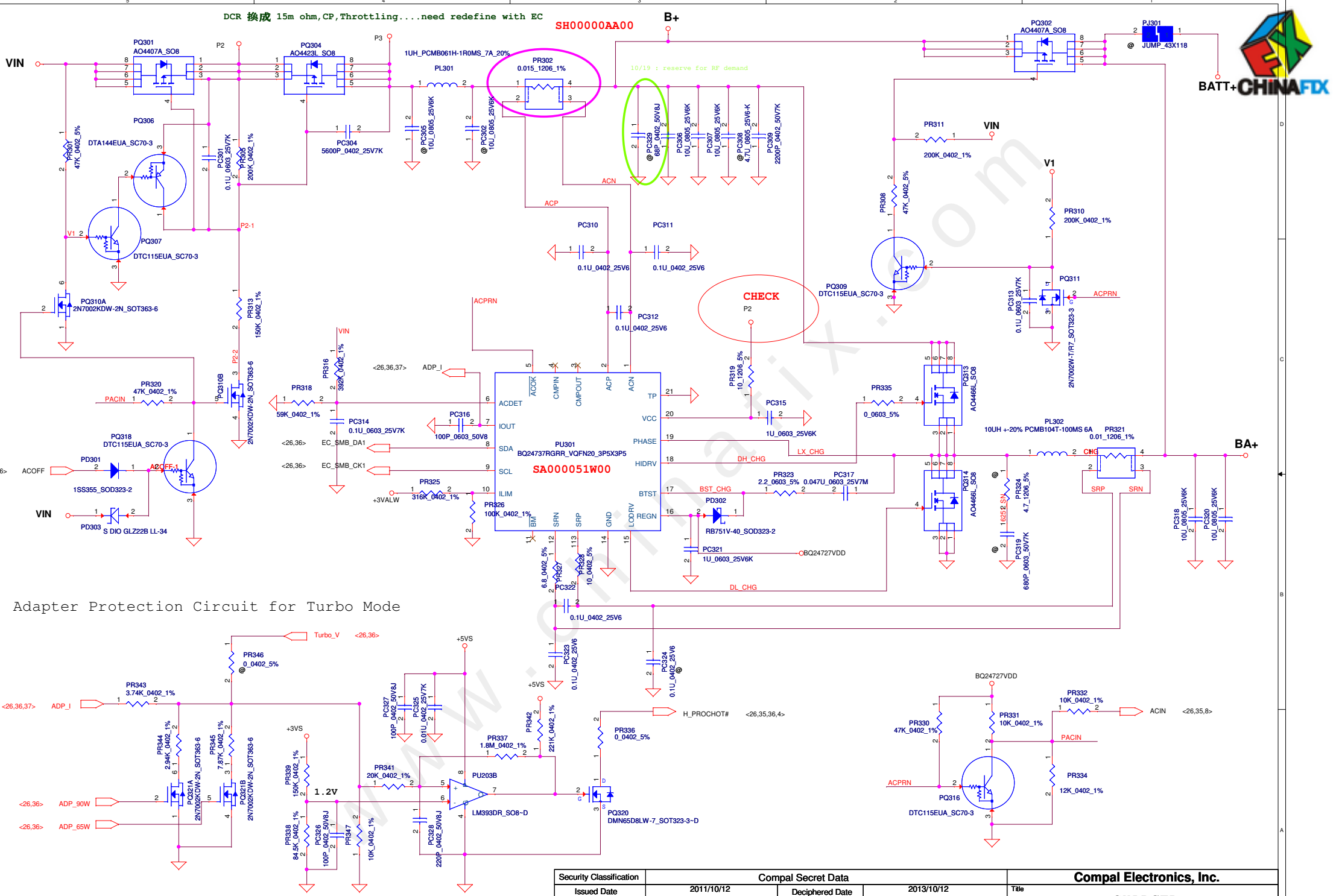

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: VIUS1 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 37 of 47

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TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)

3VALW_OCP =15.8A
Ipeak=12A

5VALW_OCP =12.7A
Ipeak=9.4A

EN
Rising=1.2-1.6- 2V
Falling0.9-0.95- 1V

<26> PWR_RESET

MAINPWON <26,32>

MOS_OTP <36>

<26> EN_5V

EN_3V <26>

2012/09/04
check the EN circuit

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Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

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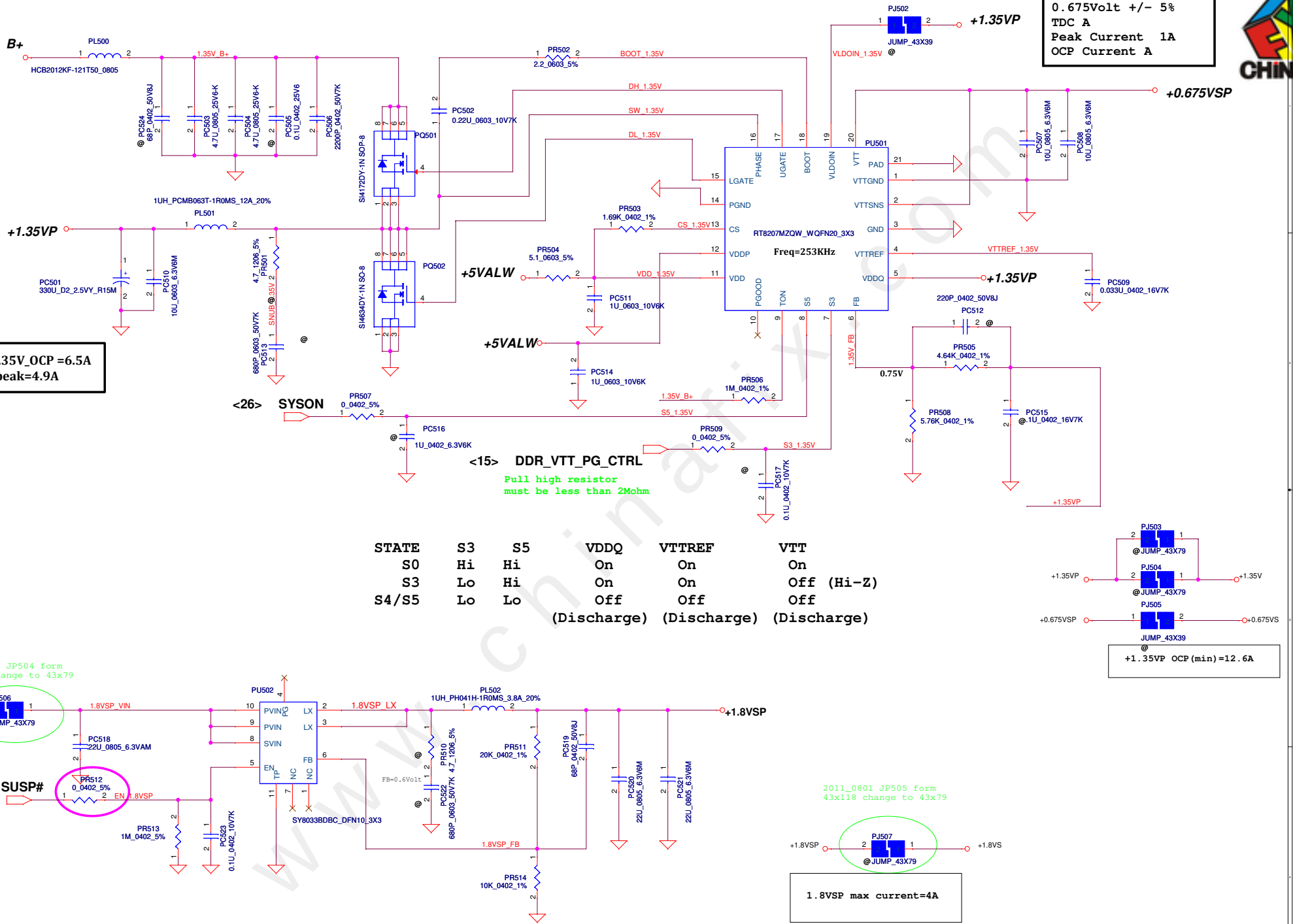
Compal Electronics, Inc.			
Title: PWR- 3VALWP/5VALWP			
Size: Custom	Document Number: VIUS1		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 38 of 47		



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR-+1.35VP/+1.8VSP

Size: Custom | Document Number: VIUS1 | Rev: 0.4

Date: Friday, November 02, 2012 | Sheet 39 of 47

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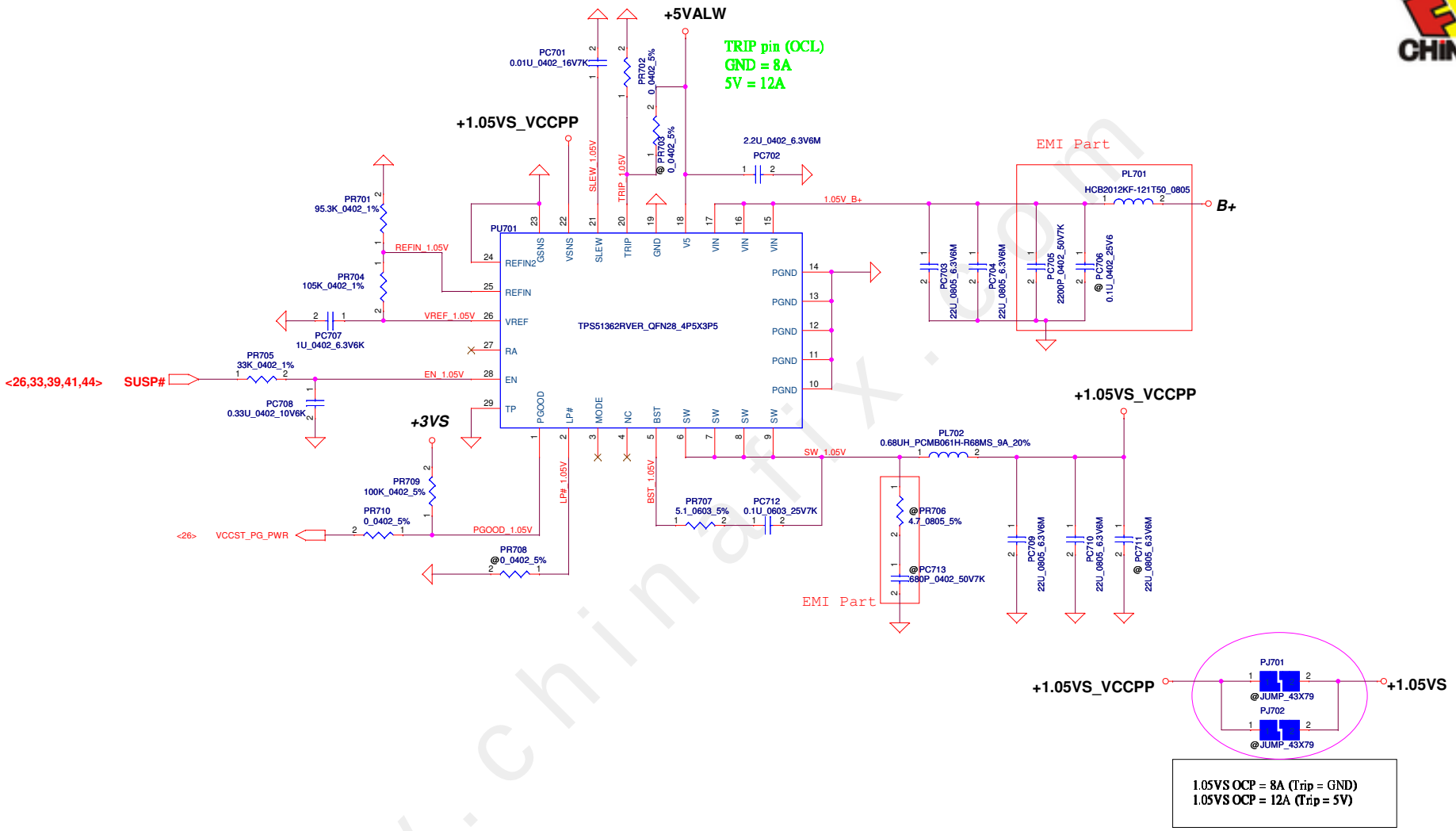

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Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

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Compal Electronics, Inc.	
Title	+1.05VS_VCCP
Size: Custom	Document Number: V5WE2 M/B LA-9531P Schematic
Rev	0.1
Date: Friday, November 02, 2012	Sheet 40 of 47

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GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

+VGA_CORE Near VGA Core

ISEN1_VGA是否要加

ISEN2_VGA是否要加

Layout Note:
Place near Phase1 Choke

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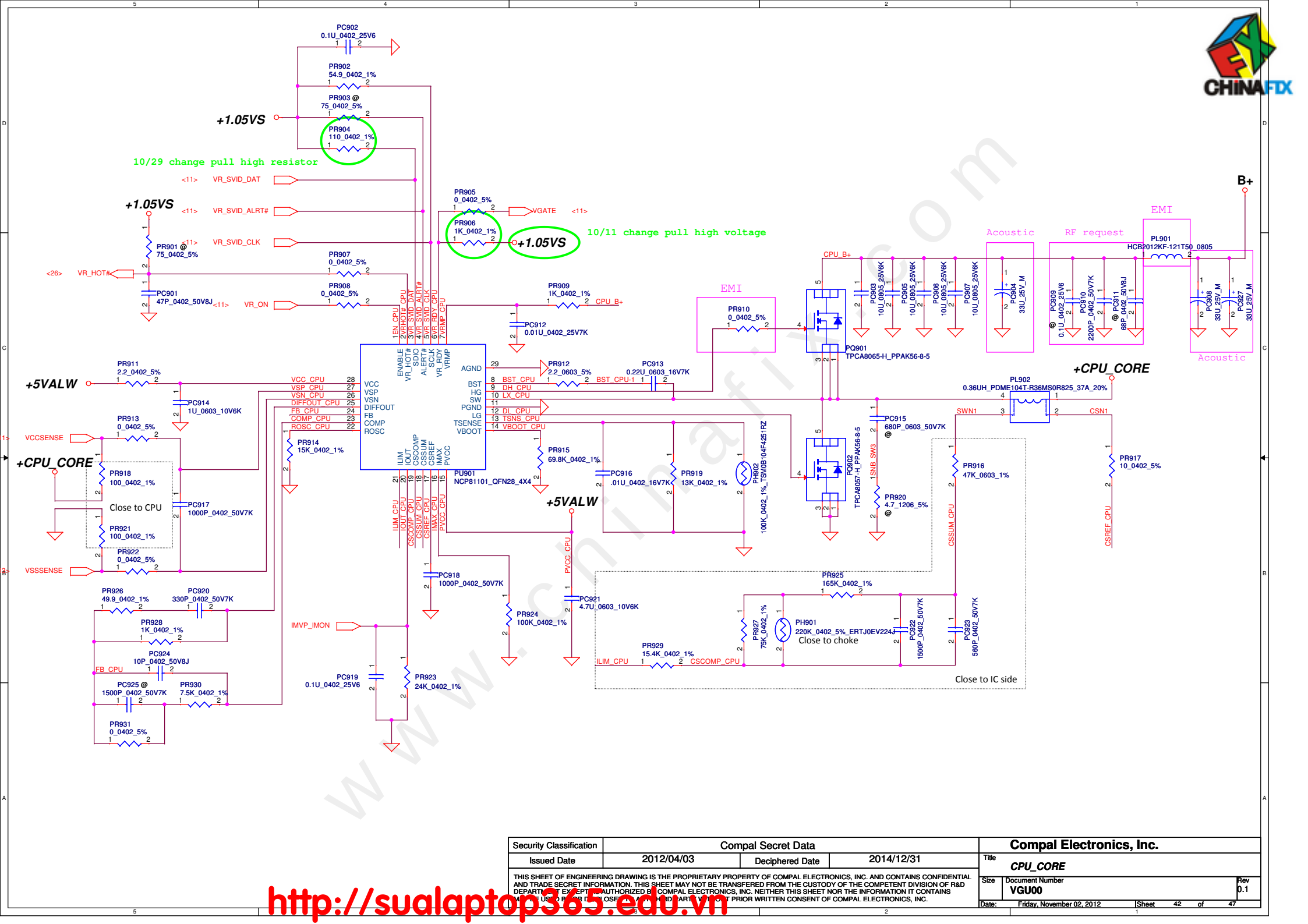
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: VGA_COREP

Size: | Document Number: VIUS1 | Rev: 0.1

Date: Friday, November 02, 2012 | Sheet 41 of 47



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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Compal Electronics, Inc.			
Title	CPU_CORE		
Size	Document Number VGU00		Rev 0.1
Date: Friday, November 02, 2012	Sheet 42 of 47		

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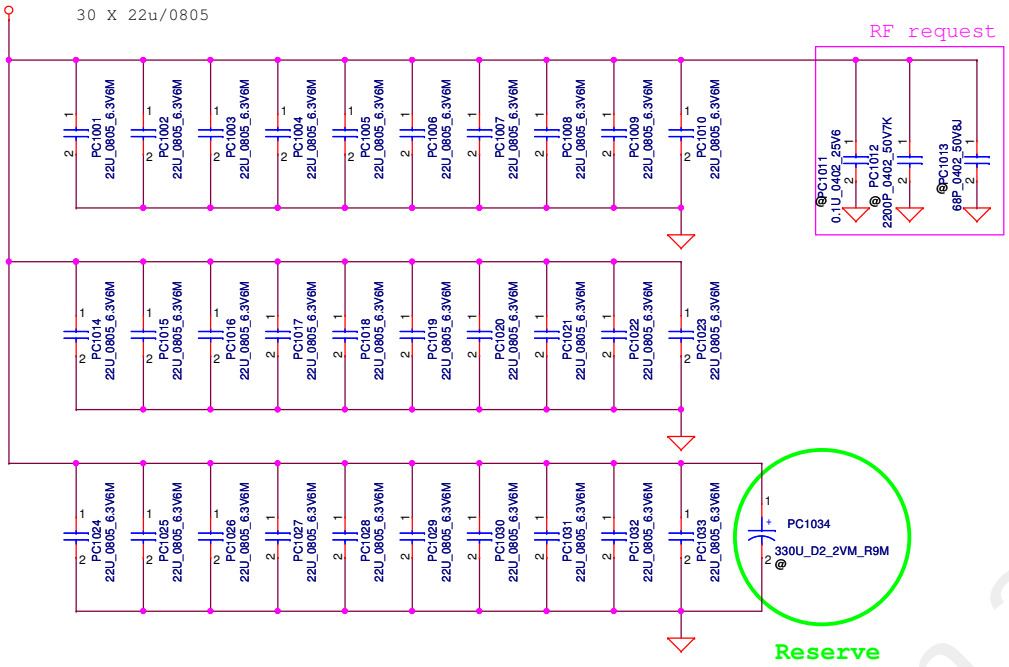
+CPU_CORE



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Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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Compal Electronics, Inc.			
Title	PROCESSOR DECOUPLING		
Size	Document Number VGU00		Rev 0.1
Date: Friday, November 02, 2012	Sheet 43 of 47		

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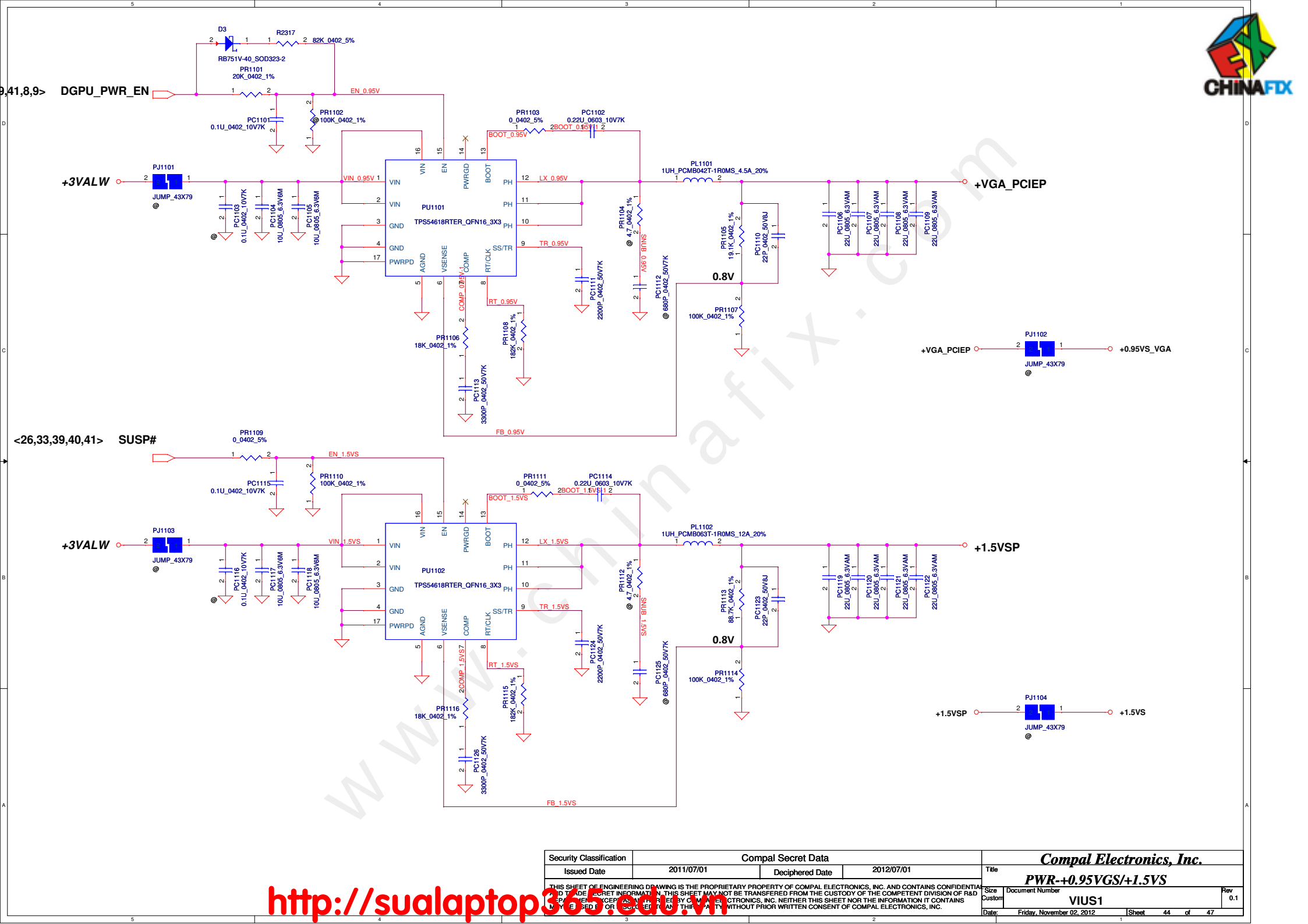

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Security Classification	Compal Secret Data		
Issued Date	2011/07/01	Deciphered Date	2012/07/01

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Compal Electronics, Inc.			
Title	PWR-+0.95VGS/+1.5VS		
Size: Custom	Document Number: VIUS1		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 44 of 47		

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1				2012/06/05	
2				2012/06/08	
3				2012/06/08	
4				2012/06/08	
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/01/06	Deciphered Date	2009/01/06
Title	PIR (PWR)		
Size: Custom	Document Number: VIUS1		Rev: 0.4
Date: Friday, November 02, 2012	Sheet 45 of 47		

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Title	PIR (EE)		
Size: Custom	Document Number: LA-8133P		Rev: 0.1
Date: Friday, November 02, 2012	Sheet 46 of 47		

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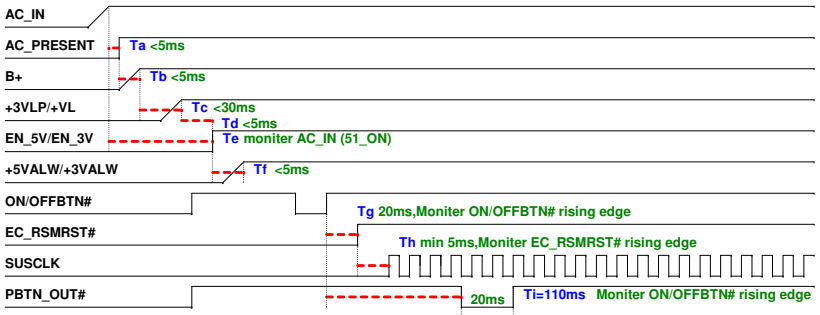

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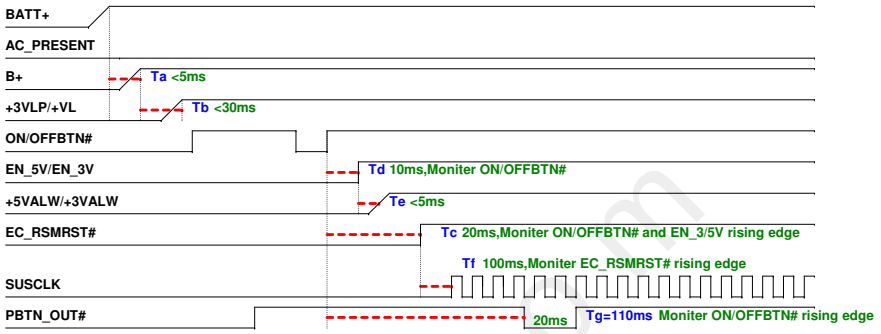

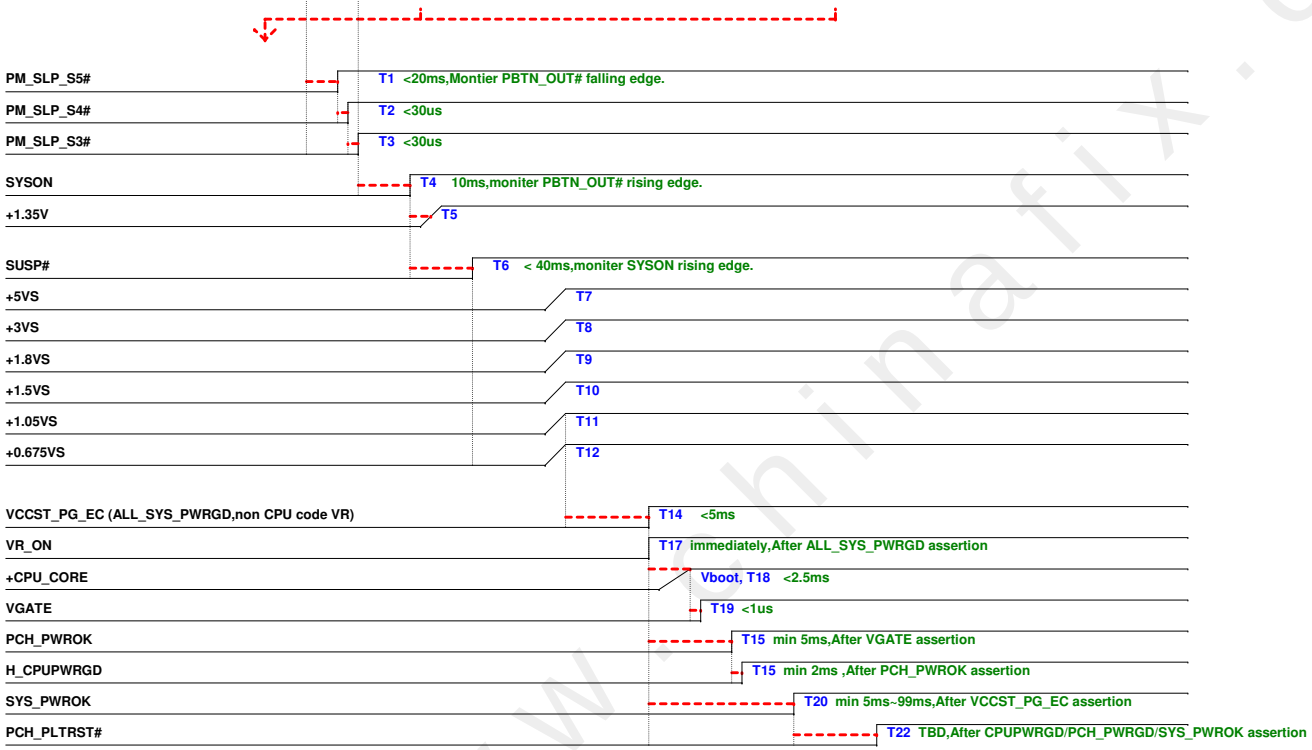

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	Power Sequence		
Size	Document Number		Rev 0.1
Date: Friday, November 02, 2012	Sheet 47 of 47		

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